

HW-Z1-ZCU102 Evaluation Board

(XCZU9EG-FFVB1156)

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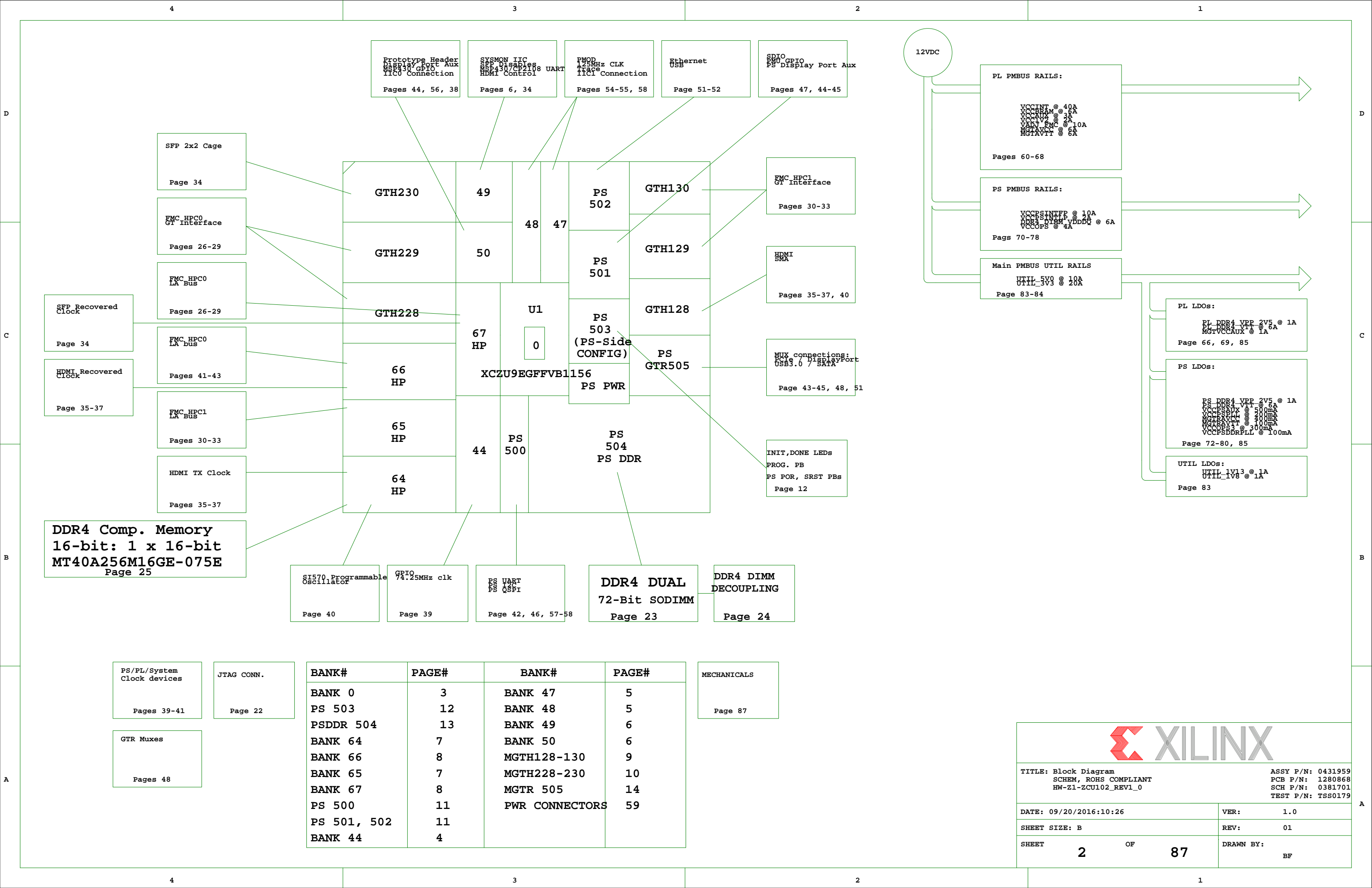
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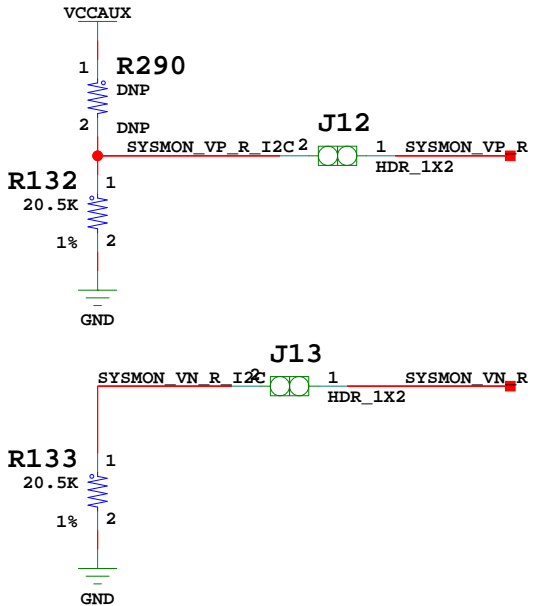
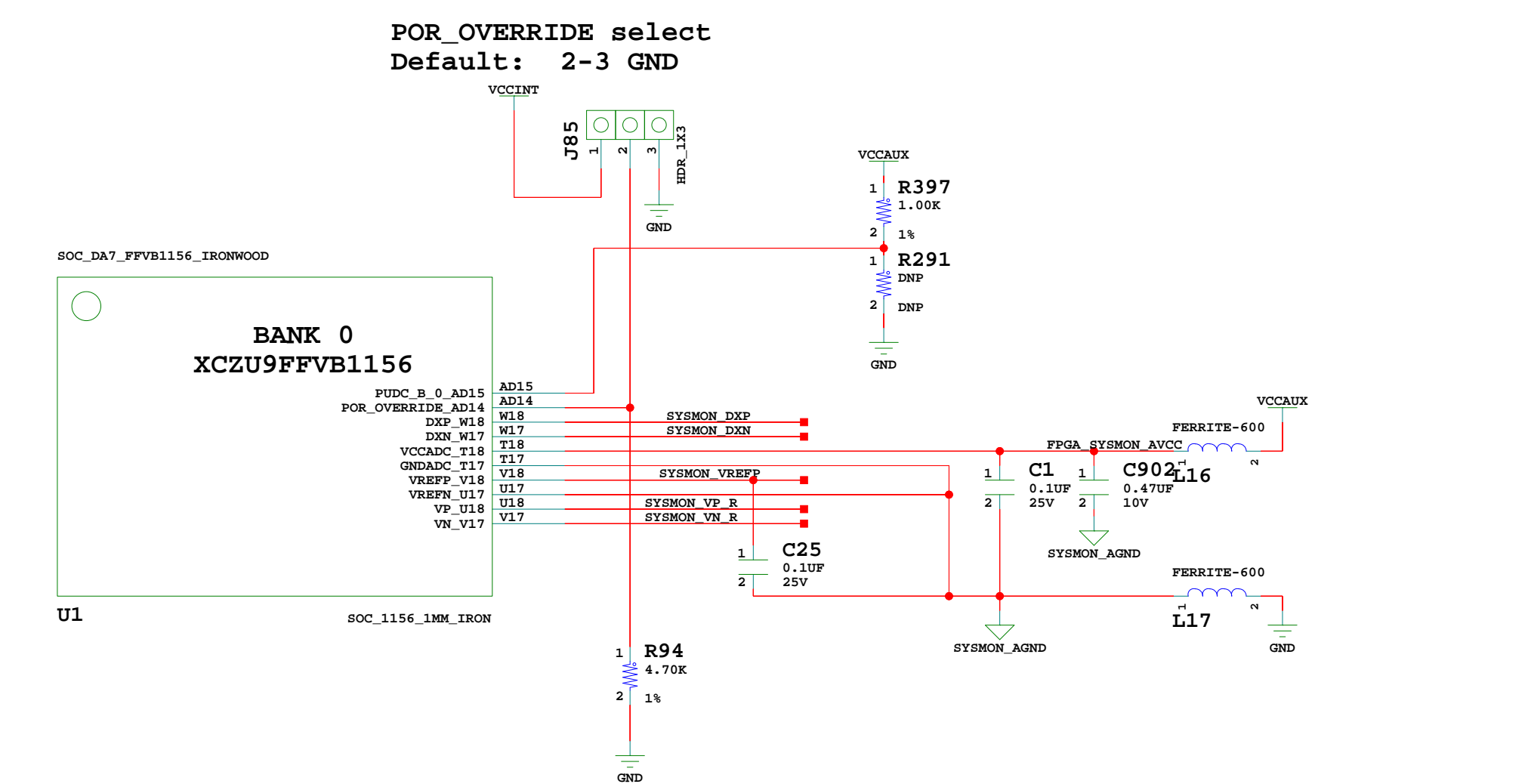
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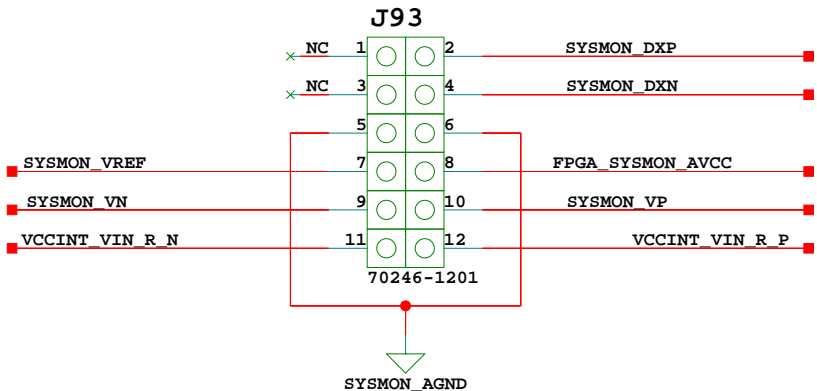
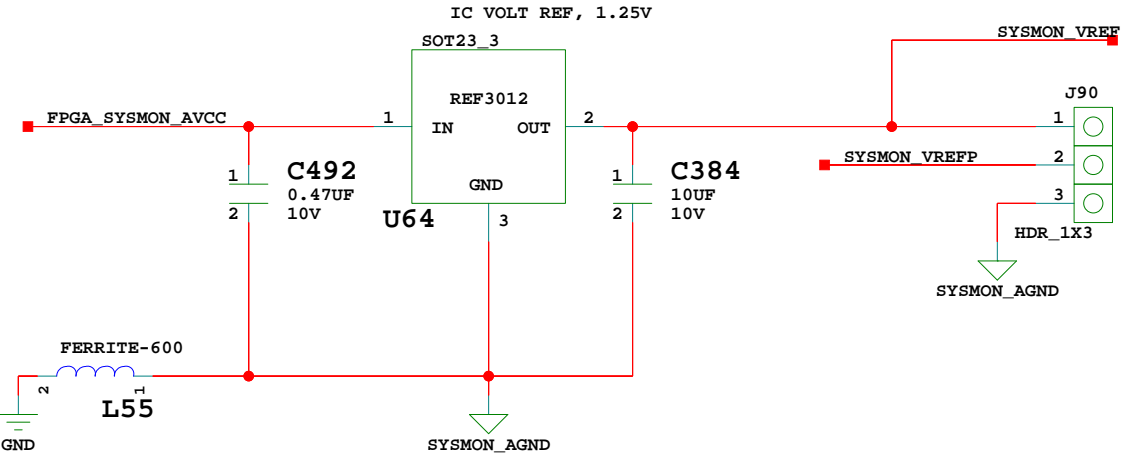
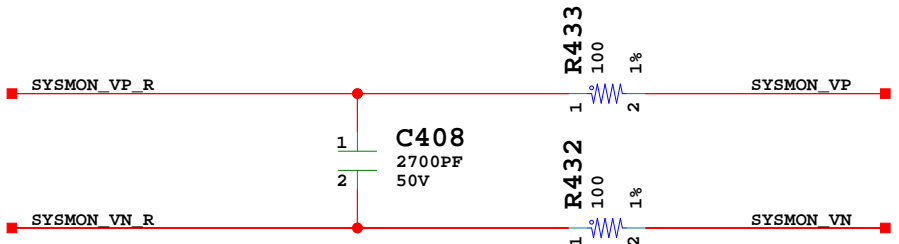
			
TITLE: Title Page		ASSY P/N: 0431959	
SCHEM, ROHS COMPLIANT		PCB P/N: 1280868	
HW-Z1-ZCU102_REV1_0		SCH P/N: 0381701	
		TEST P/N: TSS0179	
DATE: 09/20/2016:10:26		VER:	1.0
SHEET SIZE: B		REV:	01
SHEET	1	OF	87
		DRAWN BY:	BF



POR_OVERRIDE select
Default: 2-3 GND



SYSMON I2C Address jumpers



Zynq Bank 0	
TITLE: Zynq Bank 0 SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	
ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179	
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 3 OF 87	DRAWN BY: BF

SOC_DA7_FFVB1156_IRONWOOD

BANK 44
XCZU9FFVB1156

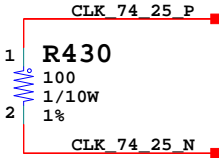
VCC3V3

AF14
AJ13

VCCO_44_AF14
VCCO_44_AJ13

IO_L12N_AD0N_44 AE14
IO_L12P_AD0P_44 AE15
IO_L11N_AD1N_44 AG15
IO_L11P_AD1P_44 AF15
IO_L10N_AD2N_44 AG13
IO_L10P_AD2P_44 AG14
IO_L9N_AD3N_44 AF13
IO_L9P_AD3P_44 AE13
IO_L8N_HDGC_AD4N_44 AJ14
IO_L8P_HDGC_AD4P_44 AJ15
IO_L7N_HDGC_AD5N_44 AH13
IO_L7P_HDGC_AD5P_44 AH14
IO_L6N_HDGC_AD6N_44 AL12
IO_L6P_HDGC_AD6P_44 AK13
IO_L5N_HDGC_AD7N_44 AK14
IO_L5P_HDGC_AD7P_44 AK15
IO_L4N_AD8N_44 AM13
IO_L4P_AD8P_44 AL13
IO_L3N_AD9N_44 AP12
IO_L3P_AD9P_44 AN12
IO_L2N_AD10N_44 AN13
IO_L2P_AD10P_44 AM14
IO_L1N_AD11N_44 AP14
IO_L1P_AD11P_44 AN14

AE14 GPIO SW E
AE15 GPIO SW S
AG15 GPIO SW N
AF15 GPIO SW W
AG13 GPIO SW C
AG14 GPIO LED 0
AF13 GPIO LED 1
AE13 GPIO LED 2
AJ14 GPIO LED 3
AJ15 GPIO LED 4
AH13 GPIO LED 5
AH14 GPIO LED 6
AL12 GPIO LED 7
AK13 GPIO DIP SW7
AK14 CLK 74 25 N
AK15 CLK 74 25 P
AM13 CPU RESET
AL13 GPIO DIP SW6
AP12 GPIO DIP SW5
AN12 GPIO DIP SW4
AN13 GPIO DIP SW3
AM14 GPIO DIP SW2
AP14 GPIO DIP SW1
AN14 GPIO DIP SW0



U1

SOC_1156_1MM_IRON

Zynq Banks 44



TITLE: Zynq Banks 44
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU102_REV1_0

ASSY P/N: 0431959
PCB P/N: 1280868
SCH P/N: 0381701
TEST P/N: TSS0179

DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 4 OF 87	DRAWN BY: BF

SOC_DA7_FFVB1156_IRONWOOD

BANK 47
XCZU9FFVB1156

IO_L12N_AD0N_47_A20
IO_L12P_AD0P_47_B20
IO_L11N_AD1N_47_A22
IO_L11P_AD1P_47_A21
IO_L10N_AD2N_47_B21
IO_L10P_AD2P_47_C21
IO_L9N_AD3N_47_C22
IO_L9P_AD3P_47_D21
IO_L8N_HDGC_AD4N_47_D20
IO_L8P_HDGC_AD4P_47_E20
IO_L7N_HDGC_AD5N_47_D22
IO_L7P_HDGC_AD5P_47_E22
IO_L6N_HDGC_AD6N_47_F20
IO_L6P_HDGC_AD6P_47_G20
IO_L5N_HDGC_AD7N_47_F21
IO_L5P_HDGC_AD7P_47_G21
IO_L4N_AD8N_47_J20
IO_L4P_AD8P_47_J19
IO_L3N_AD9N_47_H21
IO_L3P_AD9P_47_J21
IO_L2N_AD10N_47_K19
IO_L2P_AD10P_47_L19
IO_L1N_AD11N_47_K20
IO_L1P_AD11P_47_L20

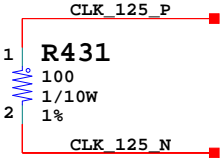
A20 PMOD0_0
B20 PMOD0_1
A22 PMOD0_2
A21 PMOD0_3
B21 PMOD0_4
C21 PMOD0_5
C22 PMOD0_6
D21 PMOD0_7
D20 PMOD1_0
E20 PMOD1_1
D22 PMOD1_2
E22 PMOD1_3
F20 PMOD1_4
G20 PMOD1_5
F21 CLK_125_N
G21 CLK_125_P
J20 PMOD1_6
J19 PMOD1_7
H21 TRACEDATA2
J21 TRACEDATA1
K19 TRACECTL
L19 TRACEDATA0
K20 PL_I2C1_SCL_LS
L20 PL_I2C1_SDA_LS

VCC3V3

E21 VCCO_47_E21
H20 VCCO_47_H20

U1

SOC_1156_1MM_IRON



SOC_DA7_FFVB1156_IRONWOOD

BANK 48
XCZU9FFVB1156

IO_L12N_AD8N_48_A18
IO_L12P_AD8P_48_A17
IO_L11N_AD9N_48_C19
IO_L11P_AD9P_48_C18
IO_L10N_AD10N_48_B19
IO_L10P_AD10P_48_B18
IO_L9N_AD11N_48_C17
IO_L9P_AD11P_48_D17
IO_L8N_HDGC_48_E18
IO_L8P_HDGC_48_E17
IO_L7N_HDGC_48_D19
IO_L7P_HDGC_48_E19
IO_L6N_HDGC_48_F18
IO_L6P_HDGC_48_F17
IO_L5N_HDGC_48_G19
IO_L5P_HDGC_48_G18
IO_L4N_AD12N_48_K17
IO_L4P_AD12P_48_L17
IO_L3N_AD13N_48_K18
IO_L3P_AD13P_48_L18
IO_L2N_AD14N_48_H17
IO_L2P_AD14P_48_J17
IO_L1N_AD15N_48_H19
IO_L1P_AD15P_48_H18

A18 TRACEDBGRQ
A17 TRACESRST_B
C19 TRACETDO
C18 TRACERTCK
B19 TRACETCK
B18 TRACETMS
C17 TRACETDI
D17 TRACETRST_B
E18 TRACEDATA15
E17 TRACEDATA14
D19 TRACEDATA13
E19 TRACEDATA12
F18 TRACEDATA11
F17 TRACEDATA10
G19 TRACEDATA9
G18 TRACEDATA8
K17 TRACECLKA
L17 TRACEDBGACK
K18 TRACEEXTTRIG
L18 TRACEDATA7
H17 TRACEDATA6
J17 TRACEDATA5
H19 TRACEDATA4
H18 TRACEDATA3

VCC3V3

G17 VCCO_48_G17
J18 VCCO_48_J18

U1

SOC_1156_1MM_IRON

Zynq Banks 47 48



TITLE: Zynq Banks 47 48
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU102_REV1_0

ASSY P/N: 0431959
PCB P/N: 1280868
SCH P/N: 0381701
TEST P/N: TSS0179

DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 5 OF 87	DRAWN BY: BF

SOC_DA7_FFVB1156_IRONWOOD

BANK 49
XCZU9FFVB1156

IO_L12N_AD8N_49_E13
IO_L12P_AD8P_49_F13
IO_L11N_AD9N_49_D12
IO_L11P_AD9P_49_E12
IO_L10N_AD10N_49_B12
IO_L10P_AD10P_49_C12
IO_L9N_AD11N_49_A12
IO_L9P_AD11P_49_A13
IO_L8N_HDGC_49_B13
IO_L8P_HDGC_49_C13
IO_L7N_HDGC_49_B14
IO_L7P_HDGC_49_C14
IO_L6N_HDGC_49_D14
IO_L6P_HDGC_49_E14
IO_L5N_HDGC_49_D15
IO_L5P_HDGC_49_E15
IO_L4N_AD12N_49_A15
IO_L4P_AD12P_49_B15
IO_L3N_AD13N_49_A16
IO_L3P_AD13P_49_B16
IO_L2N_AD14N_49_C16
IO_L2P_AD14P_49_D16
IO_L1N_AD15N_49_F15
IO_L1P_AD15P_49_F16

E13
F13
D12
E12
B12
C12
A12
A13
B13
C13
B14
C14
D14
E14
D15
E15
A15
B15
A16
B16
C16
D16
F15
F16

UART2_TXD_O_FPGA_RXD
UART2_RXD_I_FPGA_TXD
UART2_RTS_O_B
UART2_CTS_I_B
MSP430_UCAL_TXD
MSP430_UCAL_RXD
SFP0_TX_DISABLE
SFP1_TX_DISABLE
SFP2_TX_DISABLE
SFP3_TX_DISABLE
SYSMON_SDA
SYSMON_SCL
HDMI_RX_PWR_DET
HDMI_RX_HPD
HDMI_RX_CEC_SINK
HDMI_RX_SNK_SCT
HDMI_RX_SNK_SDA
HDMI_TX_EN
HDMI_TX_CEC
HDMI_TX_HPD
HDMI_TX_SRC_SCL
HDMI_TX_SRC_SDA
HDMI_CTL_SCL
HDMI_CTL_SDA

VCC3V3

E16
F14
VCCO_49_E16
VCCO_49_F14

U1

SOC_1156_1MM_IRON

VCC3V3_BUS

1
2
1
2
1
2
1
2

R633
2.00K
1/16W
1%

R632
2.00K
1/16W
1%

R631
2.00K
1/16W
1%

R630
2.00K
1/16W
1%

1
2
1
2

R894
DNP
DNP
DNP

R893
DNP
DNP
DNP

SOC_DA7_FFVB1156_IRONWOOD

BANK 50
XCZU9FFVB1156

IO_L12N_AD8N_50_J15
IO_L12P_AD8P_50_J16
IO_L11N_AD9N_50_G16
IO_L11P_AD9P_50_H16
IO_L10N_AD10N_50_H14
IO_L10P_AD10P_50_J14
IO_L9N_AD11N_50_G14
IO_L9P_AD11P_50_G15
IO_L8N_HDGC_50_G13
IO_L8P_HDGC_50_H13
IO_L7N_HDGC_50_H12
IO_L7P_HDGC_50_J12
IO_L6N_HDGC_50_F11
IO_L6P_HDGC_50_F12
IO_L5N_HDGC_50_G11
IO_L5P_HDGC_50_H11
IO_L4N_AD12N_50_D10
IO_L4P_AD12P_50_D11
IO_L3N_AD13N_50_E10
IO_L3P_AD13P_50_F10
IO_L2N_AD14N_50_G10
IO_L2P_AD14P_50_H10
IO_L1N_AD15N_50_J10
IO_L1P_AD15P_50_J11

J15
J16
G16
H16
H14
J14
G14
G15
G13
H13
H12
J12
F11
F12
G11
H11
D10
D11
E10
F10
G10
H10
J10
J11

L12N_AD8N_50_N
L12P_AD8P_50_P
L11N_AD9N_50_N
L11P_AD9P_50_P
L10N_AD10N_50_N
L10P_AD10P_50_P
L9N_AD11N_50_N
L9P_AD11P_50_P
L8N_HDGC_50_N
L8P_HDGC_50_P
HDMI_SI5324_LOL
HDMI_SI5324_RST
HDMI_SI5324_INT_ALM
NC
NC
NC
NC
MSP430_GPIO_PL_0
MSP430_GPIO_PL_1
MSP430_GPIO_PL_2
MSP430_GPIO_PL_3
SFP_SI5328_INT_ALM
PL_I2C0_SCL_LS
PL_I2C0_SDA_LS

VCC3V3

G12
J13
VCCO_50_G12
VCCO_50_J13

U1

SOC_1156_1MM_IRON

Zynq Banks 49 50



TITLE: Zynq Banks 49 50
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU102_REV1_0

ASSY P/N: 0431959
PCB P/N: 1280868
SCH P/N: 0381701
TEST P/N: TSS0179

DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 6 OF 87	DRAWN BY: BF

Layout: Place resistor and capacitor for VREF

Underneath the FPGA via array
right next to the via

SOC_DA7_FFVB1156_IRONWOOD

BANK 64
XCZU9FFVB1156

IO_T3U_N12_64_AP1
IO_L24N_T3U_N11_64_AK2
IO_L24P_T3U_N10_64_AK3
IO_L23N_T3U_N9_64_AL1
IO_L23P_T3U_N8_64_AK1
IO_L22N_T3U_N7_DBC_AD0N_64_AL2
IO_L22P_T3U_N6_DBC_AD0P_64_AL3
IO_L21N_T3L_N5_AD8N_64_AN1
IO_L21P_T3L_N4_AD8P_64_AM1
IO_L20N_T3L_N3_AD1N_64_AP3
IO_L20P_T3L_N2_AD1P_64_AN3
IO_L19N_T3L_N1_DBC_AD9N_64_AP2
IO_L19P_T3L_N0_DBC_AD9P_64_AN2
IO_T2U_N12_64_AM3
IO_L18N_T2U_N11_AD2N_64_AK4
IO_L18P_T2U_N10_AD2P_64_AK5
IO_L17N_T2U_N9_AD10N_64_AN4
IO_L17P_T2U_N8_AD10P_64_AM4
IO_L16N_T2U_N7_QBC_AD3N_64_AP6
IO_L16P_T2U_N6_QBC_AD3P_64_AN6
IO_L15N_T2L_N5_AD11N_64_AP4
IO_L15P_T2L_N4_AD11P_64_AP5
IO_L14N_T2L_N3_GC_64_AM5
IO_L14P_T2L_N2_GC_64_AM6
IO_L13N_T2L_N1_GC_QBC_64_AL5
IO_L13P_T2L_N0_GC_QBC_64_AL6
IO_T1U_N12_64_AJ7
IO_L12N_T1U_N11_GC_64_AL7
IO_L12P_T1U_N10_GC_64_AL8
IO_L11N_T1U_N9_GC_64_AK7
IO_L11P_T1U_N8_GC_64_AK8
IO_L10N_T1U_N7_QBC_AD4N_64_AP7
IO_L10P_T1U_N6_QBC_AD4P_64_AN7
IO_L9N_T1L_N5_AD12N_64_AK9
IO_L9P_T1L_N4_AD12P_64_AJ9
IO_L8N_T1L_N3_AD5N_64_AM8
IO_L8P_T1L_N2_AD5P_64_AM9
IO_L7N_T1L_N1_QBC_AD13N_64_AP8
IO_L7P_T1L_N0_QBC_AD13P_64_AN8
IO_T0U_N12_VRP_64_AN11
IO_L6N_T0U_N11_AD6N_64_AK10
IO_L6P_T0U_N10_AD6P_64_AJ10
IO_L5N_T0U_N9_AD14N_64_AP9
IO_L5P_T0U_N8_AD14P_64_AN9
IO_L4N_T0U_N7_DBC_AD7N_64_AP10
IO_L4P_T0U_N6_DBC_AD7P_64_AP11
IO_L3N_T0L_N5_AD15N_64_AM10
IO_L3P_T0L_N4_AD15P_64_AL10
IO_L2N_T0L_N3_64_AM11
IO_L2P_T0L_N2_64_AL11
IO_L1N_T0L_N1_DBC_64_AK12
IO_L1P_T0L_N0_DBC_64_AJ12
VREF_64_AJ11

AP1 DDR4_PAR
AK2 DDR4_DQ8
AK3 DDR4_DQ9
AL1 DDR4_DQ10
AK1 DDR4_DQ11
AL2 DDR4_DQS1_C
AL3 DDR4_DQS1_T
AN1 DDR4_DQ12
AM1 DDR4_DQ13
AP3 DDR4_DQ14
AN3 DDR4_DQ15
AP2 DDR4_CS_B
AN2 DDR4_DM1
AM3 DDR4_CKE
AK4 DDR4_DQ0
AK5 DDR4_DQ1
AN4 DDR4_DQ2
AM4 DDR4_DQ3
AP6 DDR4_DQS0_C
AN6 DDR4_DQS0_T
AP4 DDR4_DQ4
AP5 DDR4_DQ5
AM5 DDR4_DQ6
AM6 DDR4_DQ7
AL5 DDR4_A15_CAS_B
AL6 DDR4_DM0
AJ7 DDR4_A14_WE_B
AL7 USER_SI570_N
AL8 USER_SI570_P
AK7 DDR4_BG0
AK8 DDR4_ACT_B
AP7 DDR4_CK_C
AN7 DDR4_CK_T
AK9 DDR4_ODT
AJ9 DDR4_A16_RAS_B
AM8 DDR4_A0
AM9 DDR4_A1
AP8 DDR4_A2
AN8 DDR4_A3
AN11 VRP_64
AK10 DDR4_A4
AJ10 DDR4_A5
AP9 DDR4_A6
AN9 DDR4_A7
AP10 DDR4_A8
AP11 DDR4_A9
AM10 DDR4_A10
AL10 DDR4_A11
AM11 DDR4_A12
AL11 DDR4_A13
AK12 DDR4_BA0
AJ12 DDR4_BA1
AJ11

VADJ_FMC
AD8
AF9
AG7

SOC_DA7_FFVB1156_IRONWOOD

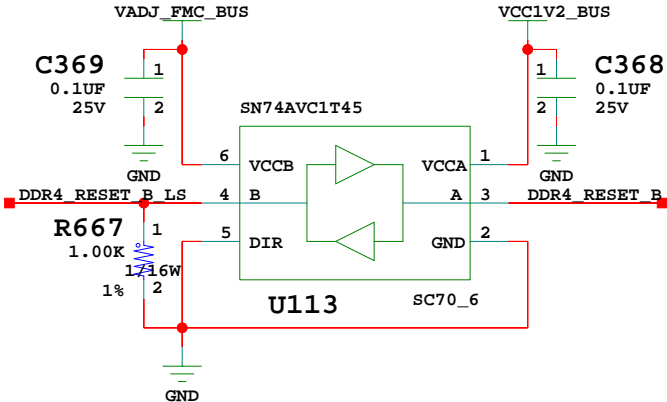
BANK 65
XCZU9FFVB1156

IO_T3U_N12_65_AG1
IO_L24N_T3U_N11_PERSTN0_65_AE1
IO_L24P_T3U_N10_PERSTN1_I2C_SDA_65_AE2
IO_L23N_T3U_N9_65_AD1
IO_L23P_T3U_N8_I2C_SCLK_65_AD2
IO_L22N_T3U_N7_DBC_AD0N_65_AJ1
IO_L22P_T3U_N6_DBC_AD0P_65_AH1
IO_L21N_T3L_N5_AD8N_65_AF1
IO_L21P_T3L_N4_AD8P_65_AF2
IO_L20N_T3L_N3_AD1N_65_AH3
IO_L20P_T3L_N2_AD1P_65_AG3
IO_L19N_T3L_N1_DBC_AD9N_65_AJ2
IO_L19P_T3L_N0_DBC_AD9P_65_AH2
IO_T2U_N12_65_AD5
IO_L18N_T2U_N11_AD2N_65_AE4
IO_L18P_T2U_N10_AD2P_65_AD4
IO_L17N_T2U_N9_AD10N_65_AF3
IO_L17P_T2U_N8_AD10P_65_AE3
IO_L16N_T2U_N7_QBC_AD3N_65_AJ5
IO_L16P_T2U_N6_QBC_AD3P_65_AJ6
IO_L15N_T2L_N5_AD11N_65_AJ4
IO_L15P_T2L_N4_AD11P_65_AH4
IO_L14N_T2L_N3_GC_65_AG4
IO_L14P_T2L_N2_GC_65_AG5
IO_L13N_T2L_N1_GC_QBC_65_AF5
IO_L13P_T2L_N0_GC_QBC_65_AE5
IO_T1U_N12_65_AH9
IO_L12N_T1U_N11_GC_65_AF7
IO_L12P_T1U_N10_GC_65_AE7
IO_L11N_T1U_N9_GC_65_AG6
IO_L11P_T1U_N8_GC_65_AF6
IO_L10N_T1U_N7_QBC_AD4N_65_AF8
IO_L10P_T1U_N6_QBC_AD4P_65_AE8
IO_L9N_T1L_N5_AD12N_65_AD6
IO_L9P_T1L_N4_AD12P_65_AD7
IO_L8N_T1L_N3_AD5N_65_AH8
IO_L8P_T1L_N2_AD5P_65_AG8
IO_L7N_T1L_N1_QBC_AD13N_65_AH6
IO_L7P_T1L_N0_QBC_AD13P_65_AH7
IO_T0U_N12_VRP_65_AD9
IO_L6N_T0U_N11_AD6N_65_AE9
IO_L6P_T0U_N10_AD6P_65_AD10
IO_L5N_T0U_N9_AD14N_65_AG9
IO_L5P_T0U_N8_AD14P_65_AG10
IO_L4N_T0U_N7_DBC_AD7N_65_AG11
IO_L4P_T0U_N6_DBC_AD7P_SMBALERT_65_AF11
IO_L3N_T0L_N5_AD15N_65_AF12
IO_L3P_T0L_N4_AD15P_65_AE12
IO_L2N_T0L_N3_65_AH11
IO_L2P_T0L_N2_65_AH12
IO_L1N_T0L_N1_DBC_65_AF10
IO_L1P_T0L_N0_DBC_65_AE10
VREF_65_AD11

VCCO_65_AD8
VCCO_65_AF9
VCCO_65_AG7

FMC_HPC1_VREF_A_M2C

R747
DNP
DNP
DNP
C968
DNP
DNP
DNP



Zynq Banks 64 65



TITLE: Zynq Banks 64 65
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU102_REV1_0
ASSY P/N: 0431959
PCB P/N: 1280868
SCH P/N: 0381701
TEST P/N: TSS0179

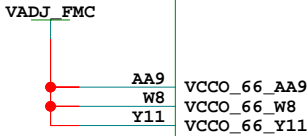
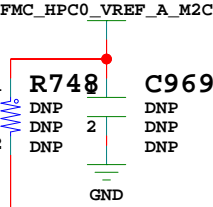
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 7 OF 87	DRAWN BY: BF

SOC_DA7_FFVB1156_IRONWOOD

BANK 66
XCZU9FFVB1156

IO_T3U_N12_66_AB1
IO_L24N_T3U_N11_66_W1
IO_L24P_T3U_N10_66_W2
IO_L23N_T3U_N9_66_V1
IO_L23P_T3U_N8_66_V2
IO_L22N_T3U_N7_DBC_AD0N_66_Y1
IO_L22P_T3U_N6_DBC_AD0P_66_Y2
IO_L21N_T3L_N5_AD8N_66_AA1
IO_L21P_T3L_N4_AD8P_66_AA2
IO_L20N_T3L_N3_AD1N_66_AC3
IO_L20P_T3L_N2_AD1P_66_AB3
IO_L19N_T3L_N1_DBC_AD9N_66_AC1
IO_L19P_T3L_N0_DBC_AD9P_66_AC2
IO_T2U_N12_66_AA3
IO_L18N_T2U_N11_AD2N_66_U4
IO_L18P_T2U_N10_AD2P_66_U5
IO_L17N_T2U_N9_AD10N_66_V3
IO_L17P_T2U_N8_AD10P_66_V4
IO_L16N_T2U_N7_QBC_AD3N_66_AC4
IO_L16P_T2U_N6_QBC_AD3P_66_AB4
IO_L15N_T2L_N5_AD11N_66_W4
IO_L15P_T2L_N4_AD11P_66_W5
IO_L14N_T2L_N3_GC_66_AA5
IO_L14P_T2L_N2_GC_66_Y5
IO_L13N_T2L_N1_GC_QBC_66_Y3
IO_L13P_T2L_N0_GC_QBC_66_Y4
IO_T1U_N12_66_AA8
IO_L12N_T1U_N11_GC_66_AA6
IO_L12P_T1U_N10_GC_66_AA7
IO_L11N_T1U_N9_GC_66_Y7
IO_L11P_T1U_N8_GC_66_Y8
IO_L10N_T1U_N7_QBC_AD4N_66_AB5
IO_L10P_T1U_N6_QBC_AD4P_66_AB6
IO_L9N_T1L_N5_AD12N_66_W6
IO_L9P_T1L_N4_AD12P_66_W7
IO_L8N_T1L_N3_AD5N_66_AC8
IO_L8P_T1L_N2_AD5P_66_AB8
IO_L7N_T1L_N1_QBC_AD13N_66_AC6
IO_L7P_T1L_N0_QBC_AD13P_66_AC7
IO_T0U_N12_VRP_66_W9
IO_L6N_T0U_N11_AD6N_66_Y9
IO_L6P_T0U_N10_AD6P_66_Y10
IO_L5N_T0U_N9_AD14N_66_AA12
IO_L5P_T0U_N8_AD14P_66_Y12
IO_L4N_T0U_N7_DBC_AD7N_66_AC9
IO_L4P_T0U_N6_DBC_AD7P_66_AB9
IO_L3N_T0L_N5_AD15N_66_AA10
IO_L3P_T0L_N4_AD15P_66_AA11
IO_L2N_T0L_N3_66_AB10
IO_L2P_T0L_N2_66_AB11
IO_L1N_T0L_N1_DBC_66_AC11
IO_L1P_T0L_N0_DBC_66_AC12
VREF_66_AD12

AB1 NC
W1 FMC HPC0 LA09 N
W2 FMC HPC0 LA09 P
V1 FMC HPC0 LA02 N
V2 FMC HPC0 LA02 P
Y1 FMC HPC0 LA03 N
Y2 FMC HPC0 LA03 P
AA1 FMC HPC0 LA04 N
AA2 FMC HPC0 LA04 P
AC3 FMC HPC0 LA05 N
AB3 FMC HPC0 LA05 P
AC1 FMC HPC0 LA06 N
AC2 FMC HPC0 LA06 P
AA3 NC
U4 FMC HPC0 LA07 N
U5 FMC HPC0 LA07 P
V3 FMC HPC0 LA08 N
V4 FMC HPC0 LA08 P
AC4 FMC HPC0 LA01 CC N
AB4 FMC HPC0 LA01 CC P
W4 FMC HPC0 LA10 N
W5 FMC HPC0 LA10 P
AA5 FMC HPC1 LA17 CC N
Y5 FMC HPC1 LA17 CC P
Y3 FMC HPC0 LA00 CC N
Y4 FMC HPC0 LA00 CC P
AA8 NC
AA6 FMC HPC0 CLK0 M2C N
AA7 FMC HPC0 CLK0 M2C P
Y7 FMC HPC1 LA18 CC N
Y8 FMC HPC1 LA18 CC P
AB5 FMC HPC0 LA11 N
AB6 FMC HPC0 LA11 P
W6 FMC HPC0 LA12 N
W7 FMC HPC0 LA12 P
AC8 FMC HPC0 LA13 N
AB8 FMC HPC0 LA13 P
AC6 FMC HPC0 LA14 N
AC7 FMC HPC0 LA14 P
W9 NC
Y9 FMC HPC0 LA15 N
Y10 FMC HPC0 LA15 P
AA12 FMC HPC0 LA16 N
Y12 FMC HPC0 LA16 P
AC9 NC
AB9 NC
AA10 FMC HPC1 LA19 N
AA11 FMC HPC1 LA19 P
AB10 FMC HPC1 LA20 N
AB11 FMC HPC1 LA20 P
AC11 FMC HPC1 LA21 N
AC12 FMC HPC1 LA21 P
AD12



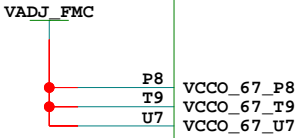
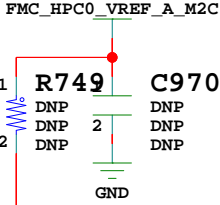
U1 SOC_1156_1MM_IRON

SOC_DA7_FFVB1156_IRONWOOD

BANK 67
XCZU9FFVB1156

IO_T3U_N12_67_K14
IO_L24N_T3U_N11_67_K15
IO_L24P_T3U_N10_67_L15
IO_L23N_T3U_N9_67_K13
IO_L23P_T3U_N8_67_L13
IO_L22N_T3U_N7_DBC_AD0N_67_M13
IO_L22P_T3U_N6_DBC_AD0P_67_N13
IO_L21N_T3L_N5_AD8N_67_N12
IO_L21P_T3L_N4_AD8P_67_P12
IO_L20N_T3L_N3_AD1N_67_M14
IO_L20P_T3L_N2_AD1P_67_M15
IO_L19N_T3L_N1_DBC_AD9N_67_K16
IO_L19P_T3L_N0_DBC_AD9P_67_L16
IO_T2U_N12_67_K10
IO_L18N_T2U_N11_AD2N_67_K12
IO_L18P_T2U_N10_AD2P_67_L12
IO_L17N_T2U_N9_AD10N_67_L11
IO_L17P_T2U_N8_AD10P_67_M11
IO_L16N_T2U_N7_QBC_AD3N_67_N8
IO_L16P_T2U_N6_QBC_AD3P_67_N9
IO_L15N_T2L_N5_AD11N_67_L10
IO_L15P_T2L_N4_AD11P_67_M10
IO_L14N_T2L_N3_GC_67_P9
IO_L14P_T2L_N2_GC_67_P10
IO_L13N_T2L_N1_GC_QBC_67_N11
IO_L13P_T2L_N0_GC_QBC_67_P11
IO_T1U_N12_67_V9
IO_L12N_T1U_N11_GC_67_R8
IO_L12P_T1U_N10_GC_67_T8
IO_L11N_T1U_N9_GC_67_R9
IO_L11P_T1U_N8_GC_67_R10
IO_L10N_T1U_N7_QBC_AD4N_67_T6
IO_L10P_T1U_N6_QBC_AD4P_67_T7
IO_L9N_T1L_N5_AD12N_67_U8
IO_L9P_T1L_N4_AD12P_67_U9
IO_L8N_T1L_N3_AD5N_67_U6
IO_L8P_T1L_N2_AD5P_67_V6
IO_L7N_T1L_N1_QBC_AD13N_67_V7
IO_L7P_T1L_N0_QBC_AD13P_67_V8
IO_T0U_N12_VRP_67_W10
IO_L6N_T0U_N11_AD6N_67_T11
IO_L6P_T0U_N10_AD6P_67_U11
IO_L5N_T0U_N9_AD14N_67_V11
IO_L5P_T0U_N8_AD14P_67_V12
IO_L4N_T0U_N7_DBC_AD7N_67_R12
IO_L4P_T0U_N6_DBC_AD7P_67_T12
IO_L3N_T0L_N5_AD15N_67_T10
IO_L3P_T0L_N4_AD15P_67_U10
IO_L2N_T0L_N3_67_R13
IO_L2P_T0L_N2_67_T13
IO_L1N_T0L_N1_DBC_67_W11
IO_L1P_T0L_N0_DBC_67_W12
VREF_67_N14

K14 NC
K15 FMC HPC0 LA26 N
L15 FMC HPC0 LA26 P
K13 FMC HPC0 LA19 N
L13 FMC HPC0 LA19 P
M13 FMC HPC0 LA20 N
N13 FMC HPC0 LA20 P
N12 FMC HPC0 LA21 N
P12 FMC HPC0 LA21 P
M14 FMC HPC0 LA22 N
M15 FMC HPC0 LA22 P
K16 FMC HPC0 LA23 N
L16 FMC HPC0 LA23 P
K10 NC
K12 FMC HPC0 LA24 N
L12 FMC HPC0 LA24 P
L11 FMC HPC0 LA25 N
M11 FMC HPC0 LA25 P
N8 FMC HPC0 LA18 CC N
N9 FMC HPC0 LA18 CC P
L10 FMC HPC0 LA27 N
M10 FMC HPC0 LA27 P
P9 FMC HPC1 CLK1 M2C N
P10 FMC HPC1 CLK1 M2C P
N11 FMC HPC0 LA17 CC N
P11 FMC HPC0 LA17 CC P
V9 NC
R8 FMC HPC0 CLK1 M2C N
T8 FMC HPC0 CLK1 M2C P
R9 SFP REC CLOCK C N
R10 SFP REC CLOCK C P
T6 FMC HPC0 LA28 N
T7 FMC HPC0 LA28 P
U8 FMC HPC0 LA29 N
U9 FMC HPC0 LA29 P
U6 FMC HPC0 LA30 N
V6 FMC HPC0 LA30 P
V7 FMC HPC0 LA31 N
V8 FMC HPC0 LA31 P
W10 NC
T11 FMC HPC0 LA32 N
U11 FMC HPC0 LA32 P
V11 FMC HPC0 LA33 N
V12 FMC HPC0 LA33 P
R12 FMC HPC1 LA26 N
T12 FMC HPC1 LA26 P
T10 FMC HPC1 LA27 N
U10 FMC HPC1 LA27 P
R13 FMC HPC1 LA28 N
T13 FMC HPC1 LA28 P
W11 FMC HPC1 LA29 N
W12 FMC HPC1 LA29 P
N14



U1 SOC_1156_1MM_IRON

Zynq Banks 66 67

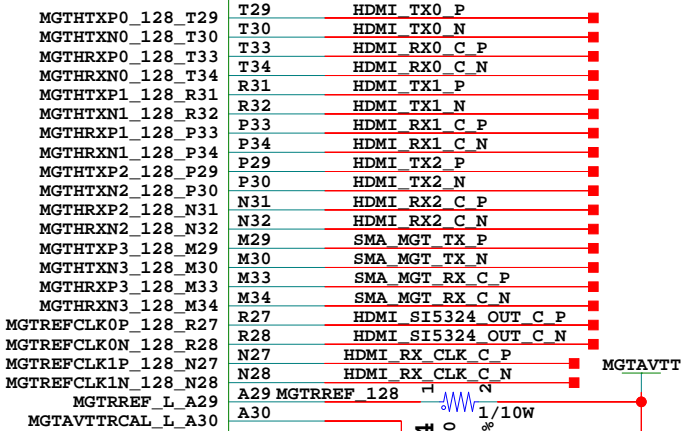


TITLE: Zynq Banks 66 67
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU102_REV1_0
ASSY P/N: 0431959
PCB P/N: 1280868
SCH P/N: 0381701
TEST P/N: TSS0179

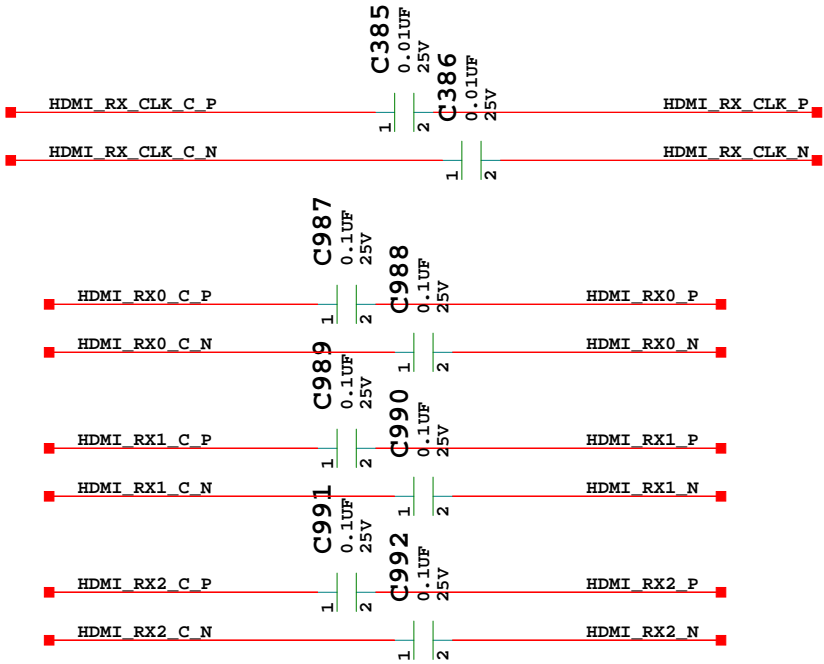
DATE: 09/20/2016:10:45	VER: 1.0
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SHEET 8 OF 87	DRAWN BY: BF

SOC_DA7_FFVB1156_IRONWOOD

BANK 128
XCZU9FFVB1156

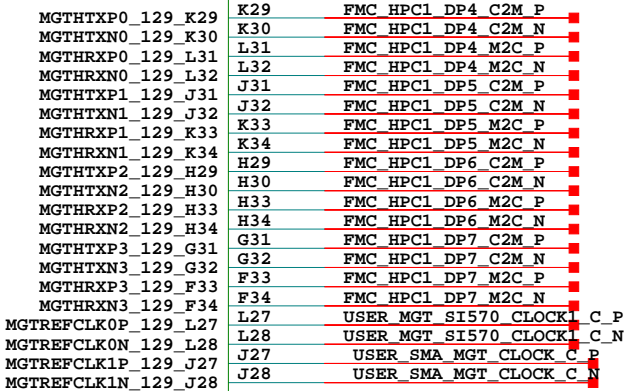


U1 SOC_1156_1MM_IRON

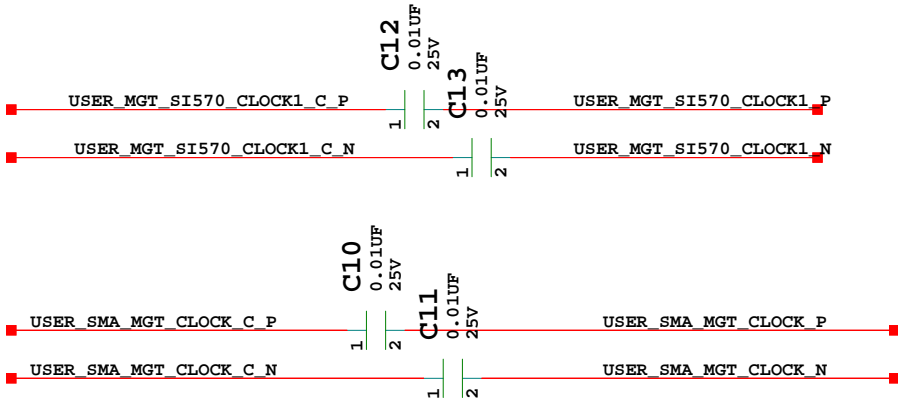


SOC_DA7_FFVB1156_IRONWOOD

BANK 129
XCZU9FFVB1156

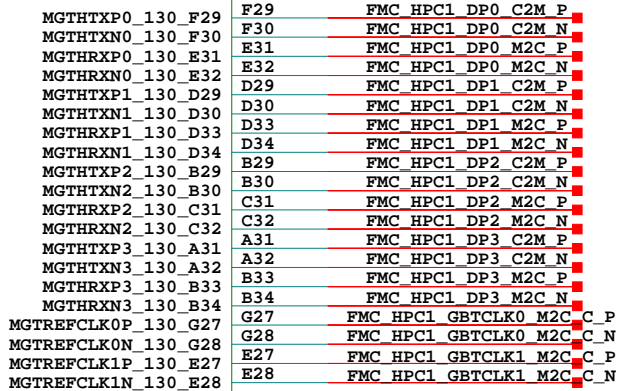


U1 SOC_1156_1MM_IRON

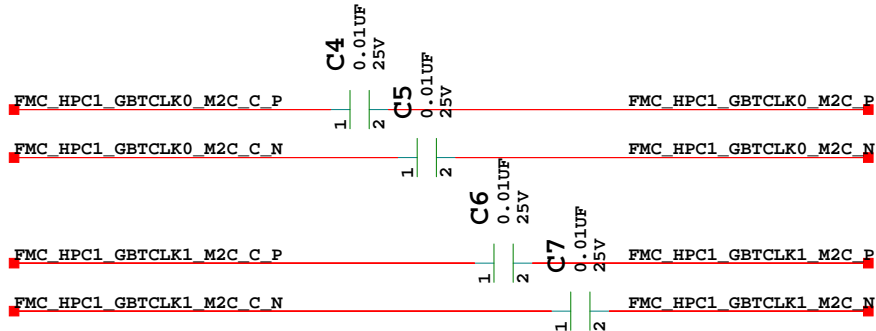


SOC_DA7_FFVB1156_IRONWOOD

BANK 130
XCZU9FFVB1156



U1 SOC_1156_1MM_IRON



Zynq Banks 128 129 130

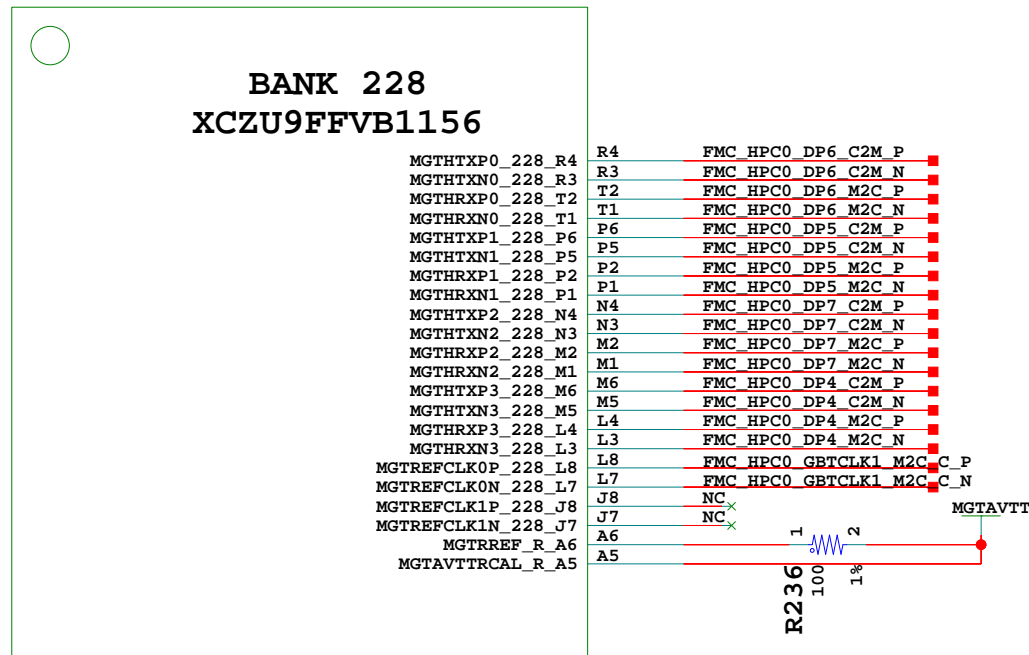


TITLE: Zynq Banks 128 129 130
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU102_REV1_0

ASSY P/N: 0431959
PCB P/N: 1280868
SCH P/N: 0381701
TEST P/N: TSS0179

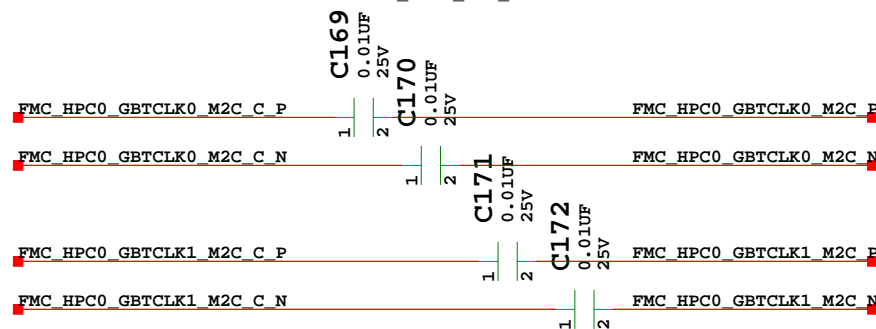
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SHEET SIZE: B	REV: 01
SHEET 9 OF 87	DRAWN BY: BF

SOC_DA7_FFVB1156_IRONWOOD

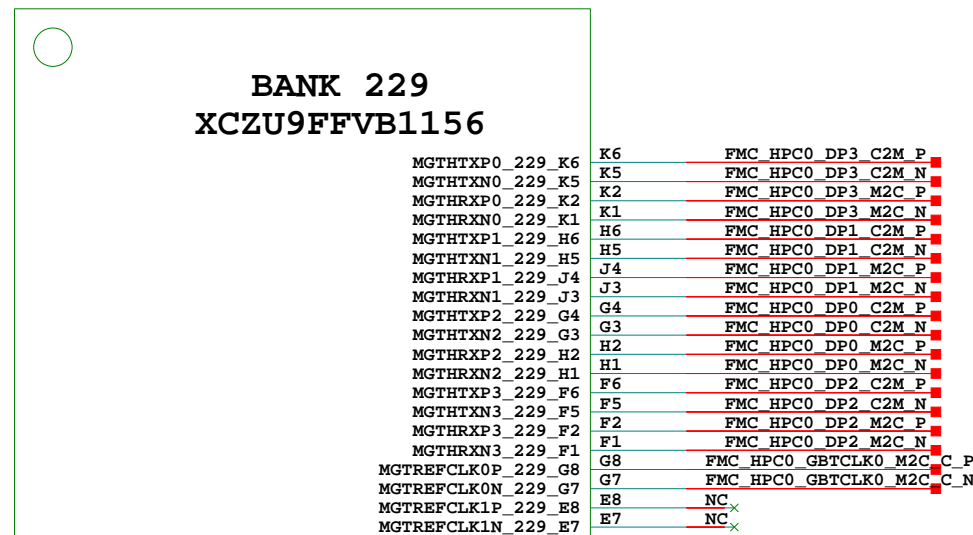


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SOC_1156_1MM_IRON



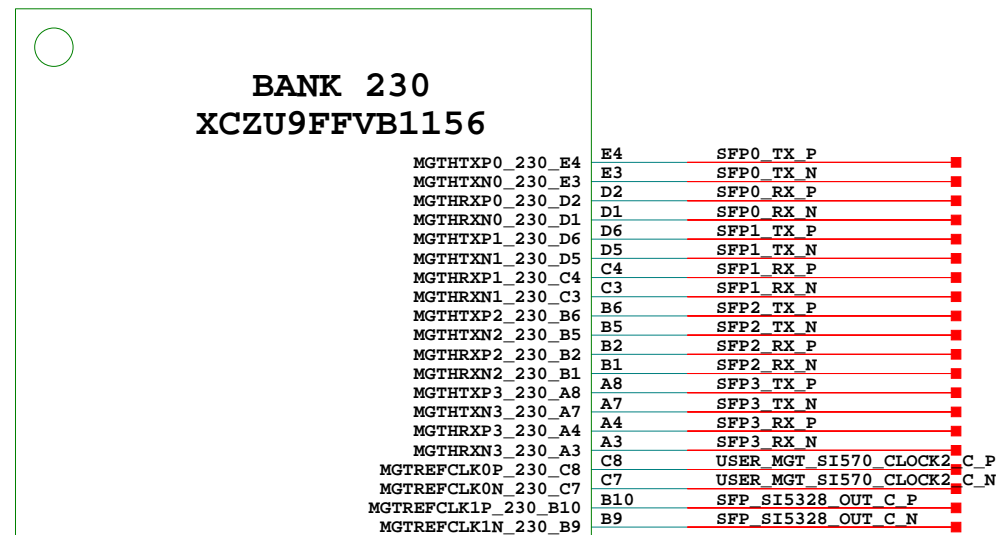
SOC_DA7_FFVB1156_IRONWOOD



U1

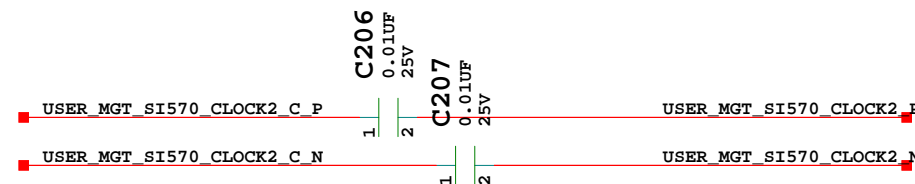
SOC 1156 1MM IRON

SOC_DA7_FFVB1156_IRONWOOD



U1

SOC 1156 1MM IRON



Zynq Banks 228 229 230



TITLE: Zynq Banks 228 229 230
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU102 REV1_0

ASSY P/N: 0431959
PCB P/N: 1280868
SCH P/N: 0381701
TEST P/N: TSS0179

DATE: 09/20/2016:10:26

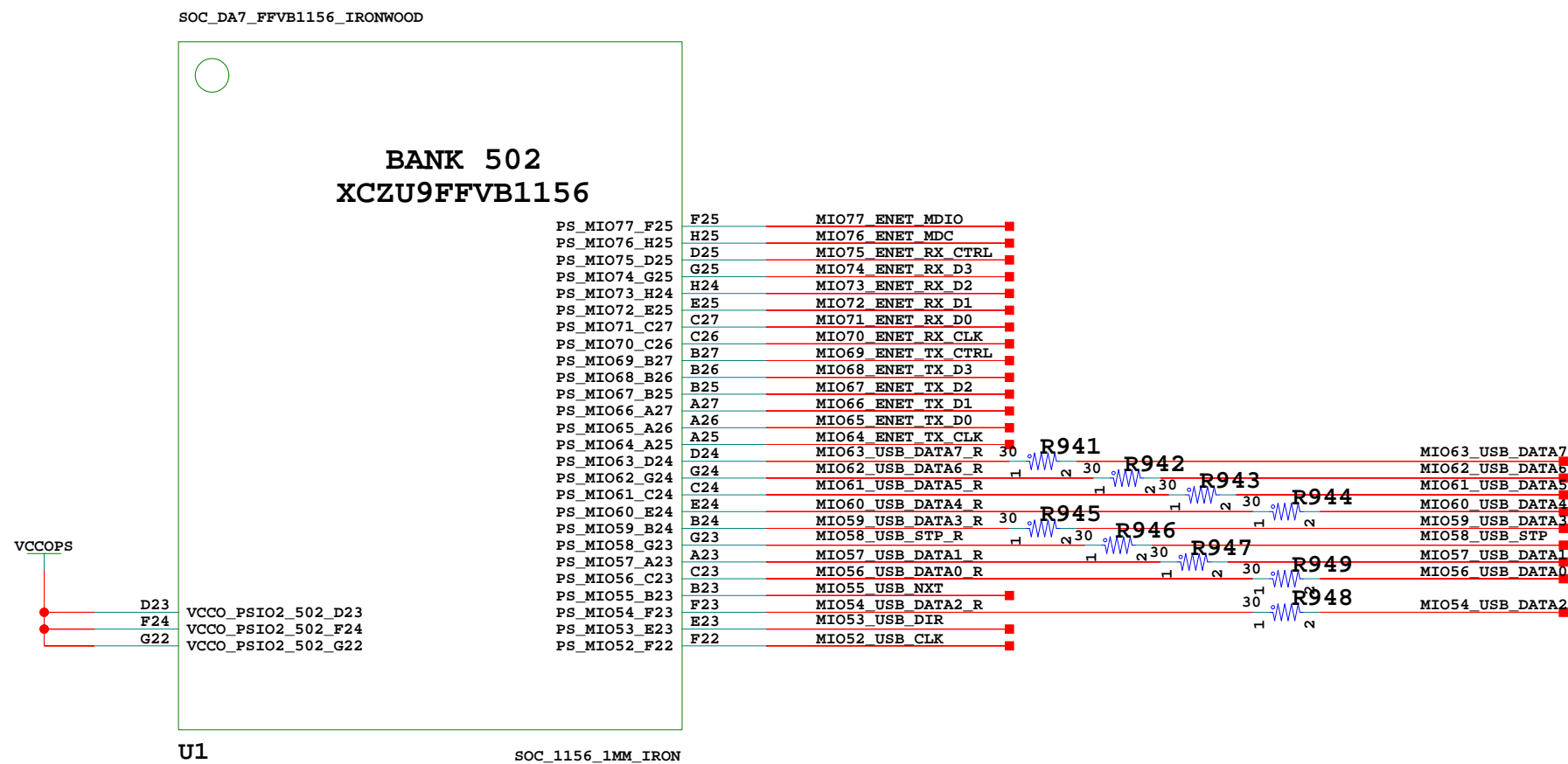
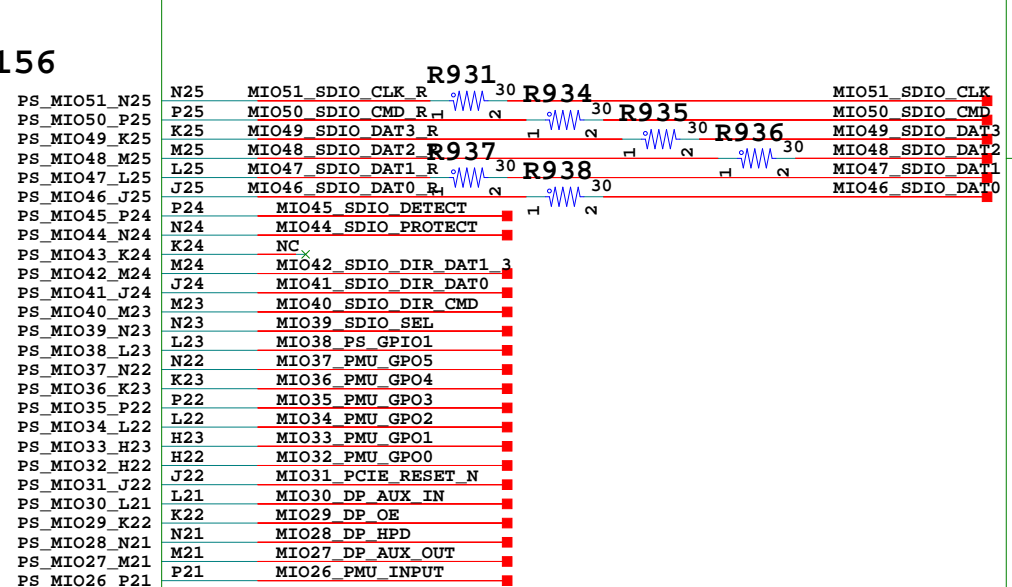
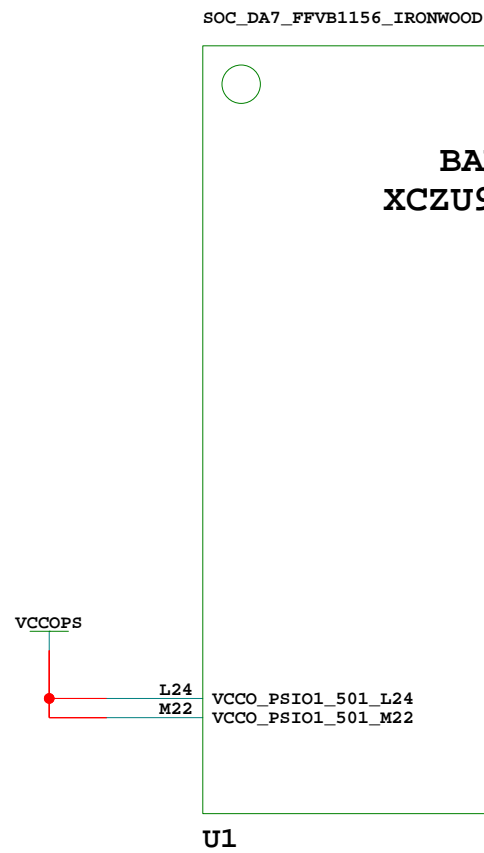
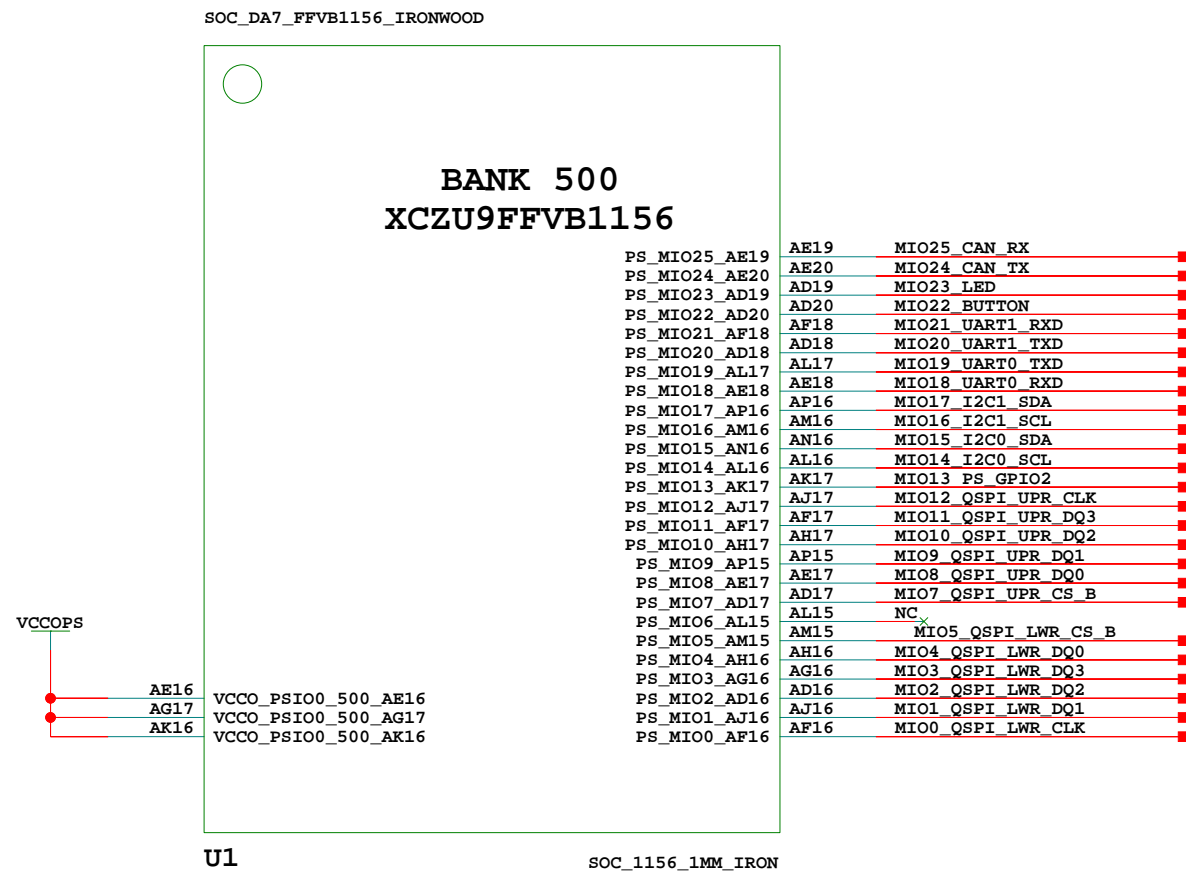
VER: 1.0

SHEET SIZE: B

REV: 01

SHEET 10 OF 87

DRAWN BY: BF

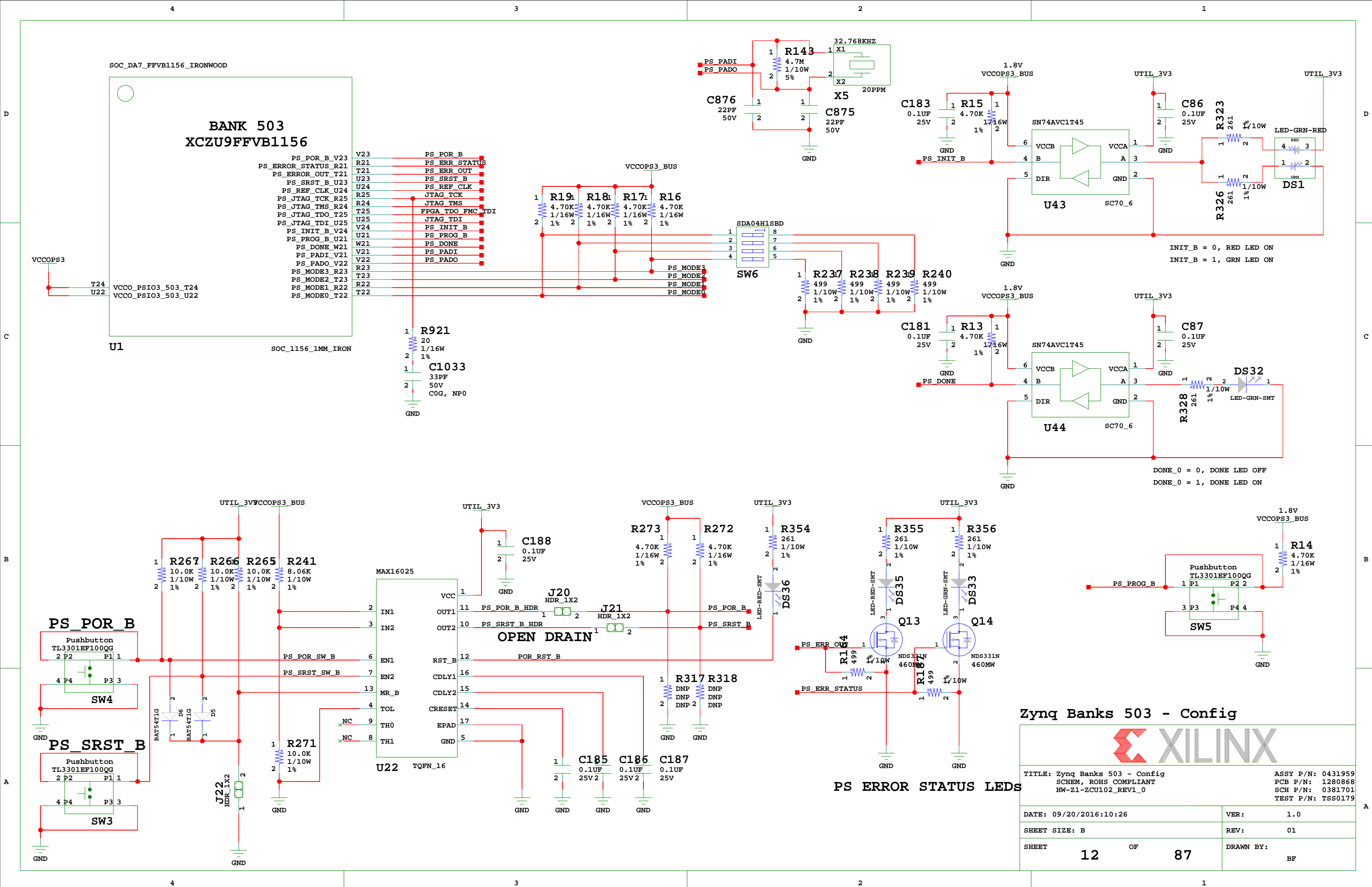


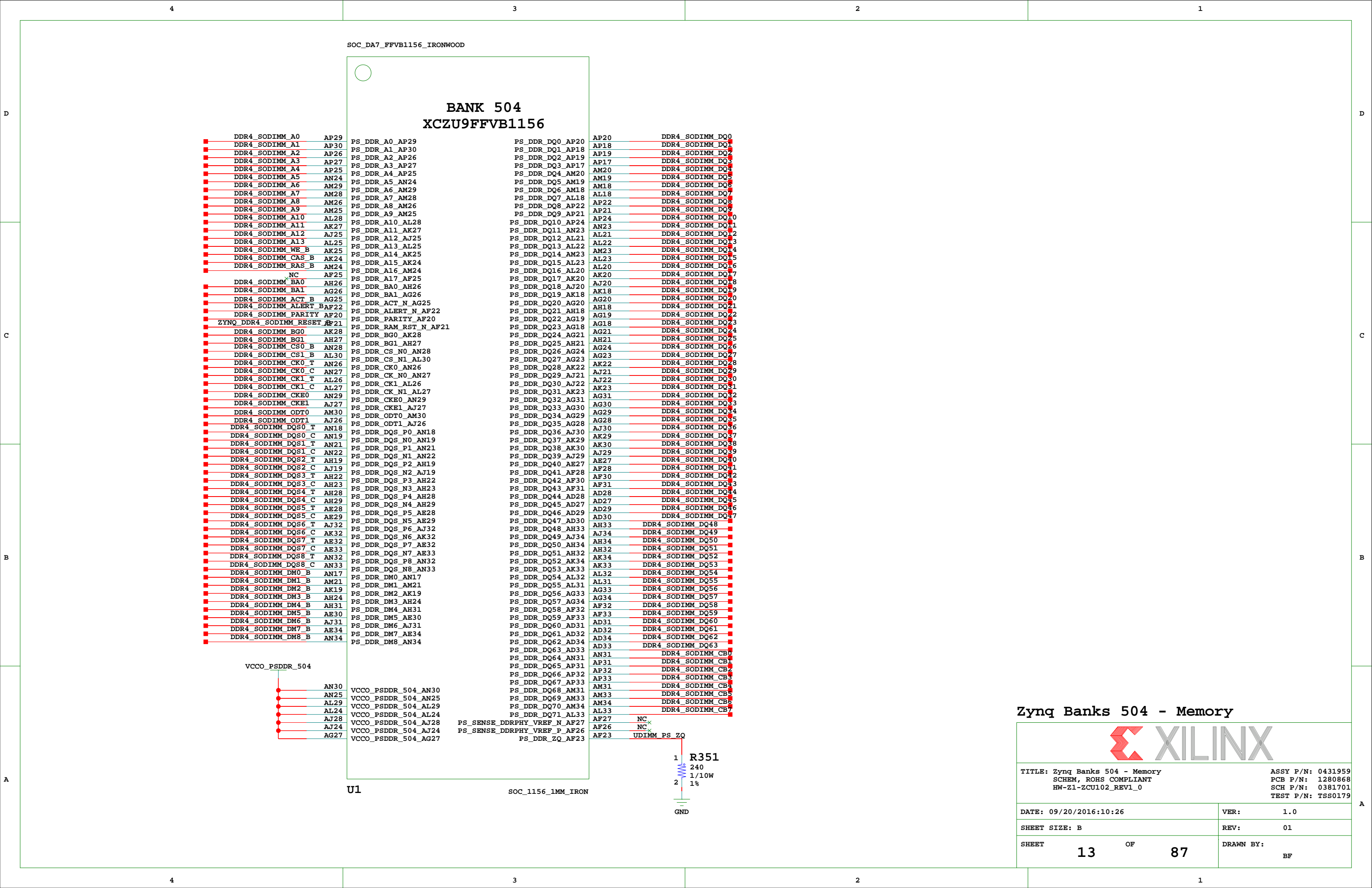
Zynq Banks 500 501 502 - MIO




TITLE: Zynq Banks 500 501 502 - MIO	ASSY P/N: 0431959
SCHEM, ROHS COMPLIANT	PCB P/N: 1280868
HW-Z1-ZCU102_REV1_0	SCH P/N: 0381701
	TEST P/N: TSS0179

DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 11 OF 87	DRAWN BY: BF





Zynq Banks 504 - Memory

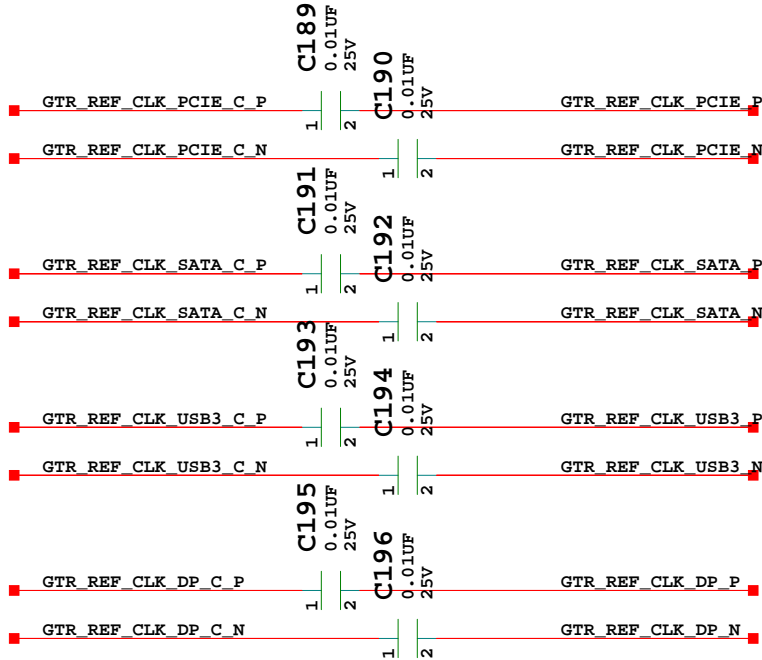
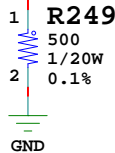
	
TITLE: Zynq Banks 504 - Memory SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	
ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179	
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 13 OF 87	DRAWN BY: BF

SOC_DA7_FFVB1156_IRONWOOD

BANK 505
XCZU9FFVB1156

PS_MGTRTXP0_505_AB29
PS_MGTRTXN0_505_AB30
PS_MGTRRXP0_505_AB33
PS_MGTRRXN0_505_AB34
PS_MGTRTXP1_505_Y29
PS_MGTRTXN1_505_Y30
PS_MGTRRXP1_505_AA31
PS_MGTRRXN1_505_AA32
PS_MGTRTXP2_505_W31
PS_MGTRTXN2_505_W32
PS_MGTRRXP2_505_Y33
PS_MGTRRXN2_505_Y34
PS_MGTRTXP3_505_V29
PS_MGTRTXN3_505_V30
PS_MGTRRXP3_505_V33
PS_MGTRRXN3_505_V34
PS_MGTREFCLK0P_505_AA27
PS_MGTREFCLK0N_505_AA28
PS_MGTREFCLK1P_505_W27
PS_MGTREFCLK1N_505_W28
PS_MGTREFCLK2P_505_U27
PS_MGTREFCLK2N_505_U28
PS_MGTREFCLK3P_505_U31
PS_MGTREFCLK3N_505_U32
PS_MGTRREF_505_AB28

AB29 GTR_LANE0_TX_P
AB30 GTR_LANE0_TX_N
AB33 GTR_LANE0_RX_P
AB34 GTR_LANE0_RX_N
Y29 GTR_LANE1_TX_P
Y30 GTR_LANE1_TX_N
AA31 GTR_LANE1_RX_P
AA32 GTR_LANE1_RX_N
W31 GTR_LANE2_TX_P
W32 GTR_LANE2_TX_N
Y33 GTR_LANE2_RX_P
Y34 GTR_LANE2_RX_N
V29 GTR_LANE3_TX_P
V30 GTR_LANE3_TX_N
V33 GTR_LANE3_RX_P
V34 GTR_LANE3_RX_N
AA27 GTR_REF_CLK_PCIE_C_P
AA28 GTR_REF_CLK_PCIE_C_N
W27 GTR_REF_CLK_SATA_C_P
W28 GTR_REF_CLK_SATA_C_N
U27 GTR_REF_CLK_USB3_C_P
U28 GTR_REF_CLK_USB3_C_N
U31 GTR_REF_CLK_DP_C_P
U32 GTR_REF_CLK_DP_C_N
AB28

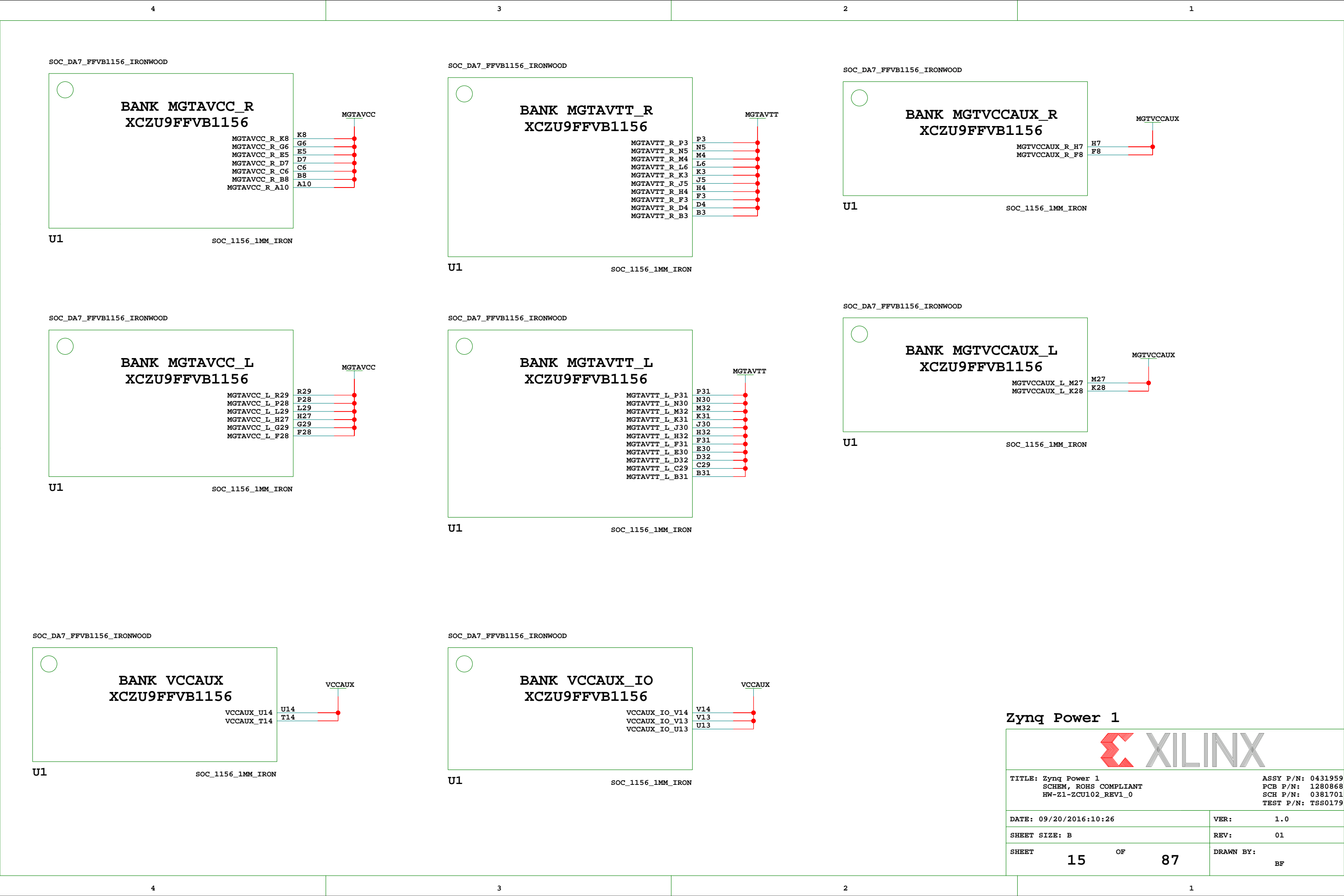


Zynq Banks 505 - GTR



TITLE: Zynq Banks 505 - GTR
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU102_REV1_0
ASSY P/N: 0431959
PCB P/N: 1280868
SCH P/N: 0381701
TEST P/N: TSS0179

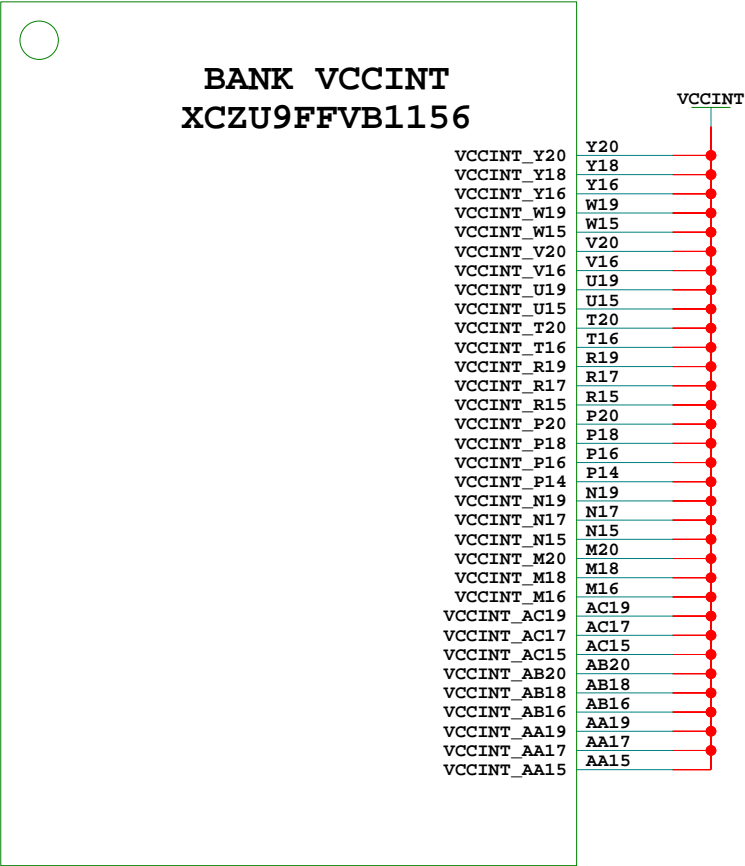
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 14 OF 87	DRAWN BY: BF



Zynq Power 1

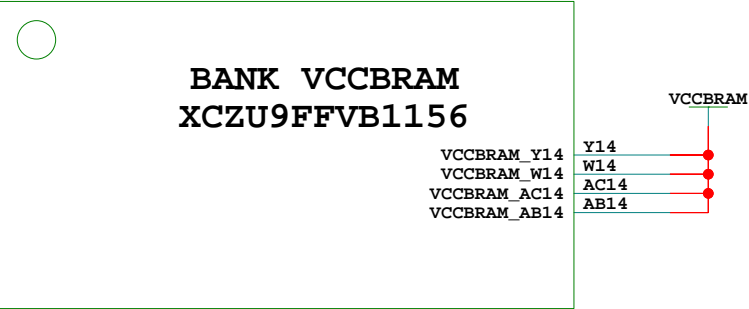
TITLE: Zynq Power 1 SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0		ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179	
DATE: 09/20/2016:10:26		VER:	1.0
SHEET SIZE: B		REV:	01
SHEET	15	OF	87
		DRAWN BY:	BF

SOC_DA7_FFVB1156_IRONWOOD



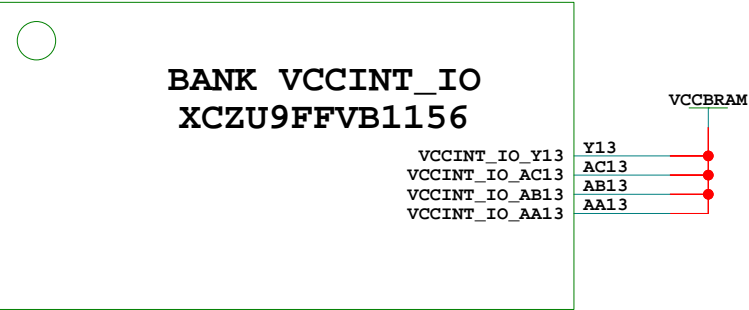
U1 SOC_1156_1MM_IRON

SOC_DA7_FFVB1156_IRONWOOD



U1 SOC_1156_1MM_IRON

SOC_DA7_FFVB1156_IRONWOOD

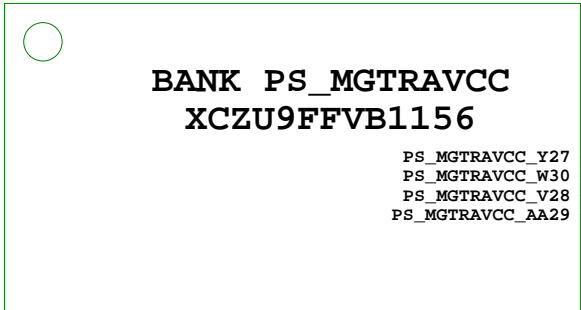


U1 SOC_1156_1MM_IRON

Zynq Power 2

TITLE: Zynq Power 2 SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0		ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179	
DATE: 09/20/2016:10:26		VER:	1.0
SHEET SIZE: B		REV:	01
SHEET	16	OF	87
		DRAWN BY:	BF

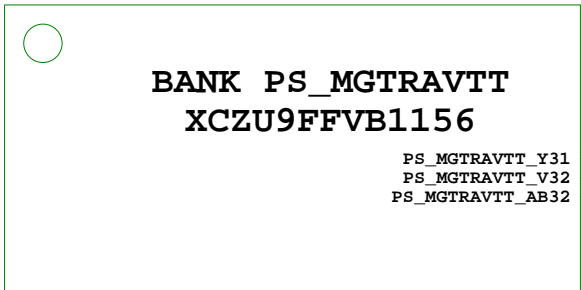
SOC_DA7_FFVB1156_IRONWOOD



U1

SOC_1156_1MM_IRON

SOC_DA7_FFVB1156_IRONWOOD



U1

SOC_1156_1MM_IRON

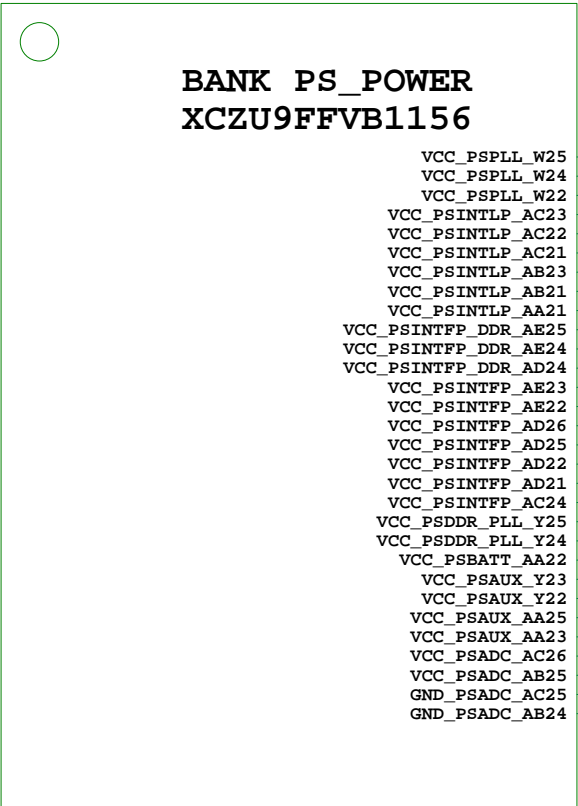
MGTRAVCC



MGTRAVTT



SOC_DA7_FFVB1156_IRONWOOD



U1

SOC_1156_1MM_IRON

VCCPSPLL

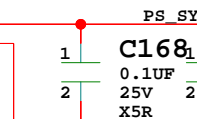
VCCPSINTLP

VCCPSINTFP

VCCPSDDRPLL

VCCPSAUX

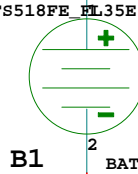
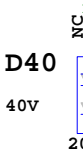
VCC_PSBATT



PS_SYSMON_AGND

PS_SYSMON_AVCC

FERRITE-600



B1

GND

UTIL_1V8

VCC_PSBATT

Zynq Power 3



TITLE: Zynq Power 3
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU102_REV1_0

ASSY P/N: 0431959
PCB P/N: 1280868
SCH P/N: 0381701
TEST P/N: TSS0179

DATE: 09/20/2016:10:26

VER: 1.0

SHEET SIZE: B

REV: 01

SHEET

17

OF

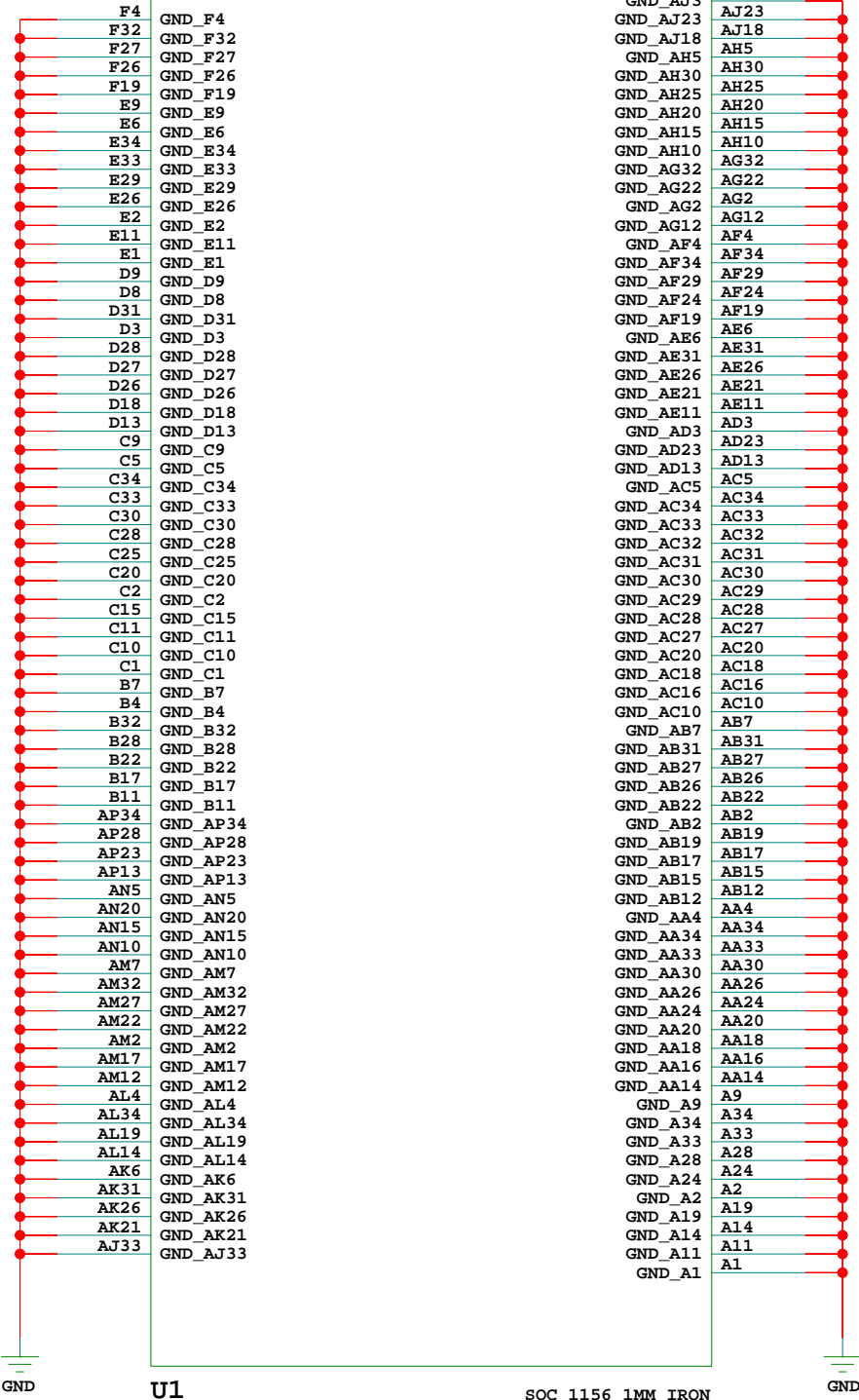
87

DRAWN BY:

BF

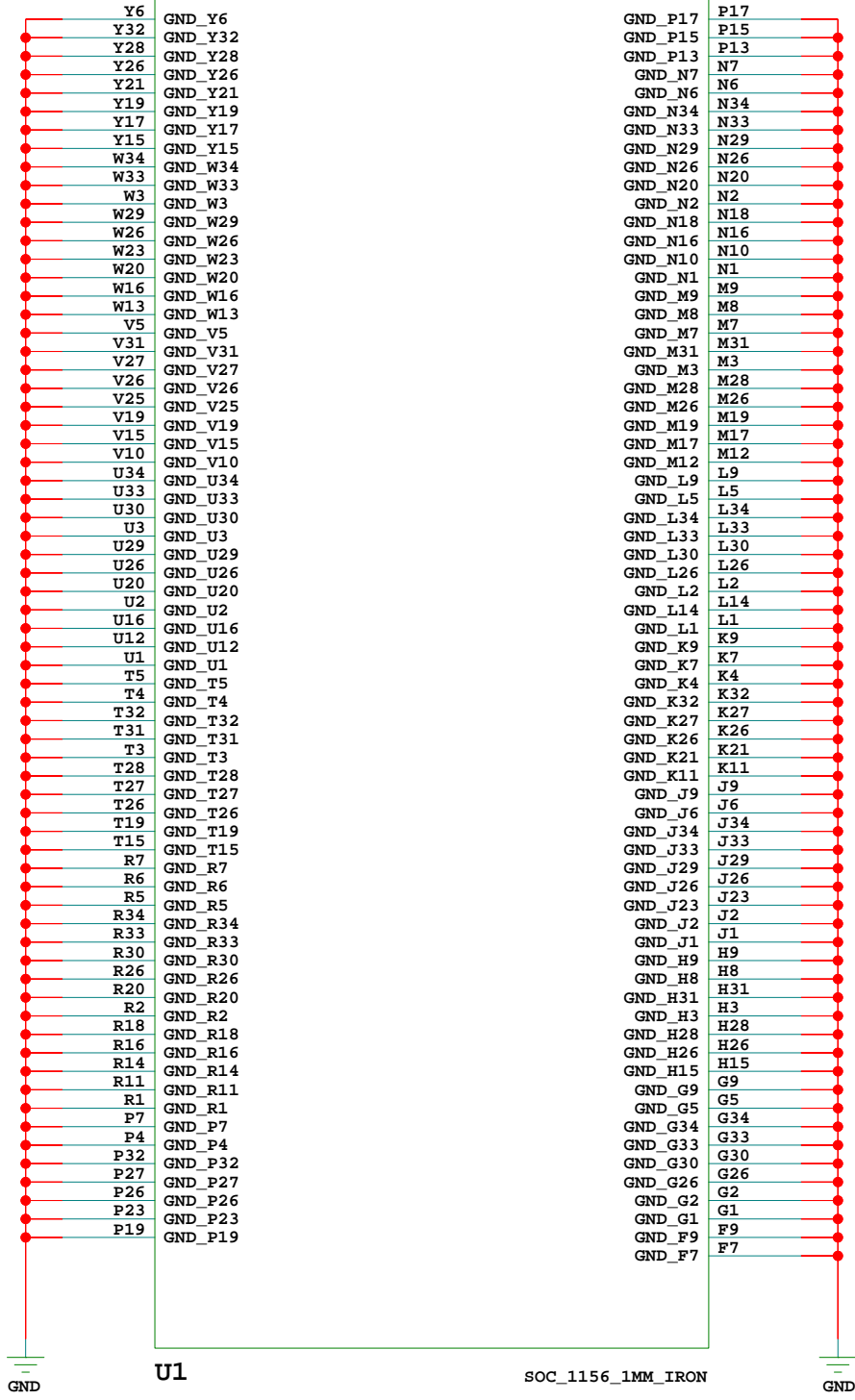
SOC_DA7_FFVB1156_IRONWOOD

BANK GND1
XCZU9FFVB1156



SOC_DA7_FFVB1156_IRONWOOD

BANK GND2
XCZU9FFVB1156



Zynq GND



TITLE: Zynq GND
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU102_REV1_0

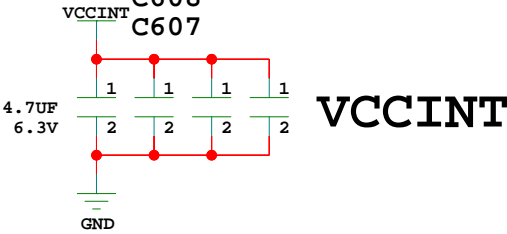
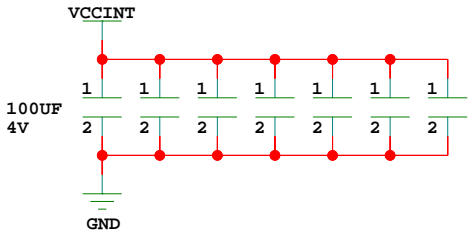
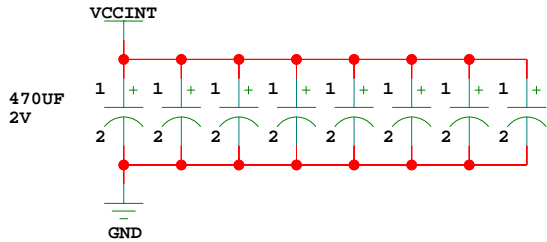
ASSY P/N: 0431959
PCB P/N: 1280868
SCH P/N: 0381701
TEST P/N: TSS0179

DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 18 OF 87	DRAWN BY: BF

C696 C700
C697 C701
C698 C702
C699 C703

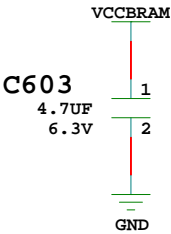
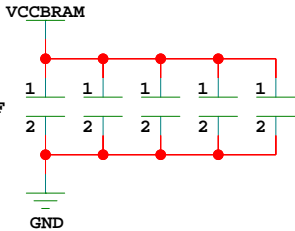
C424 C428
C425 C431
C426 C432
C427

C602
C606
C608
C607



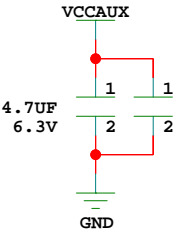
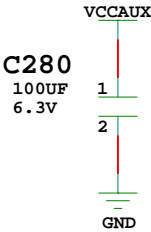
VCCINT

C934 C429
C935 C430
C933



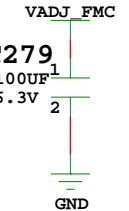
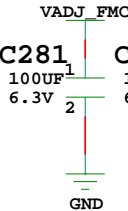
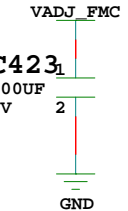
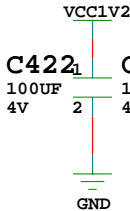
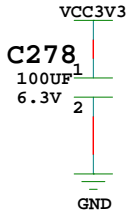
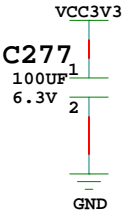
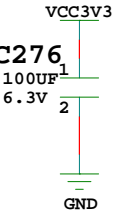
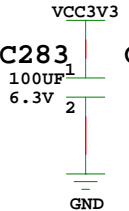
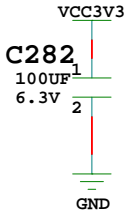
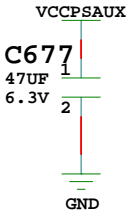
VCCBRAM

C604
C605



VCCAUX / VCCAUX_IO

VCCO BANKS 0 44 47 48 49 50 64 65 66 67



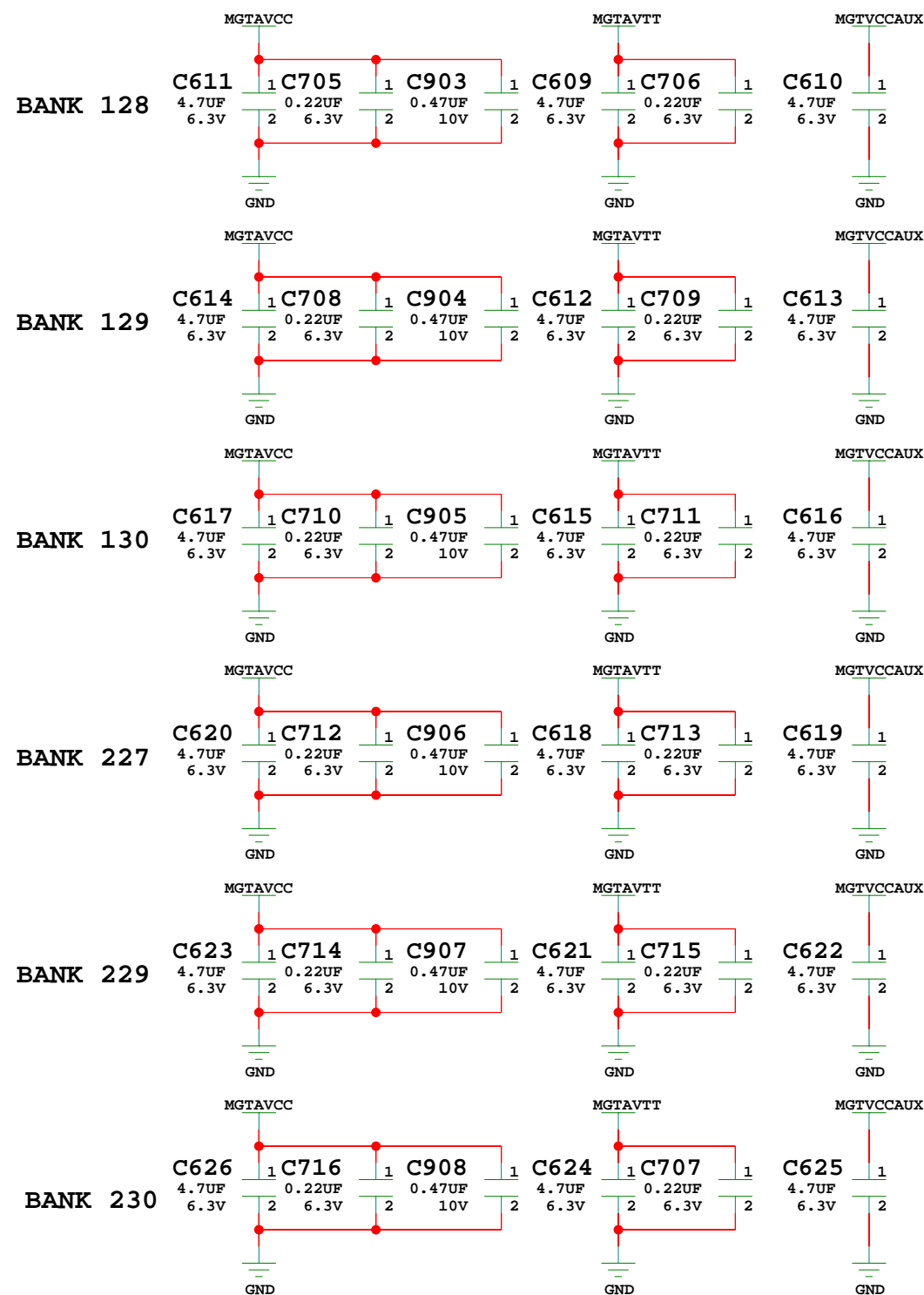
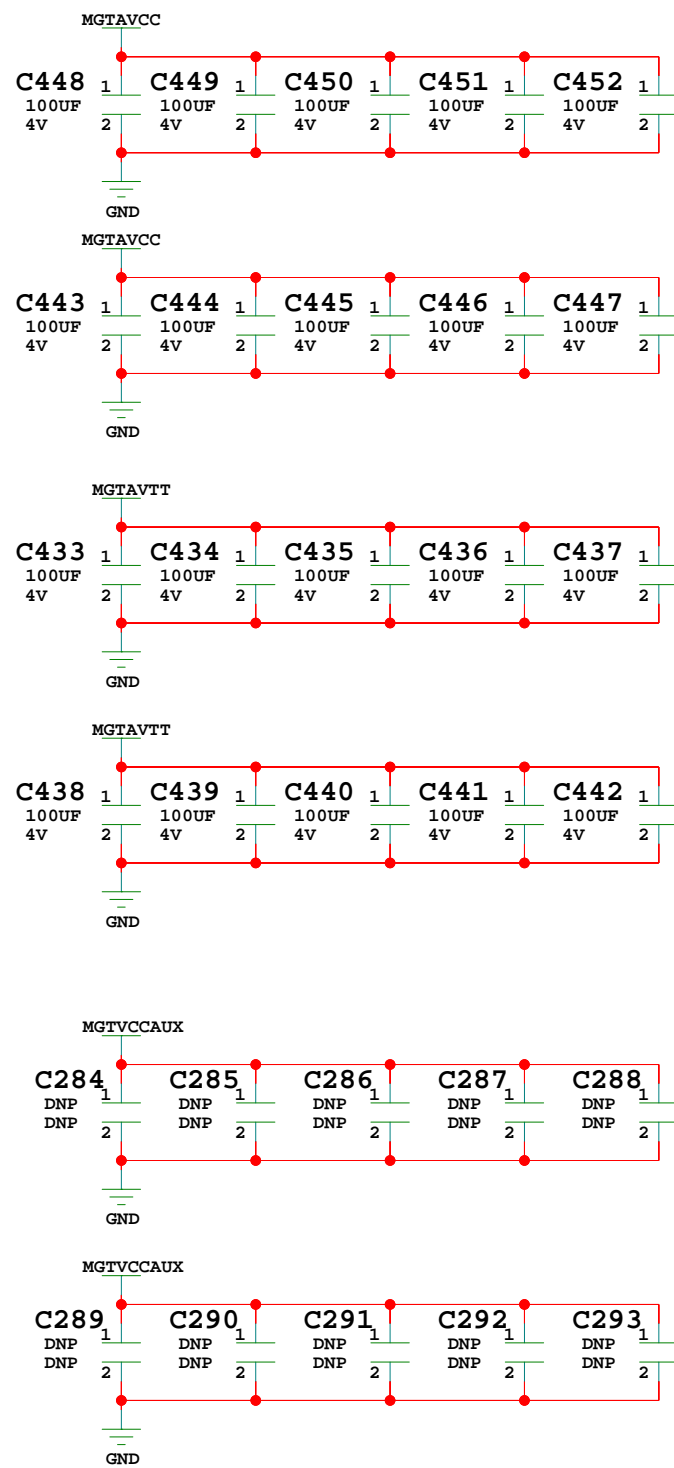
Zynq Decoupling 1



TITLE: Zynq Decoupling 1
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU102_REV1_0

ASSY P/N: 0431959
PCB P/N: 1280868
SCH P/N: 0381701
TEST P/N: TSS0179

DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 19 OF 87	DRAWN BY: BF



Zynq Decoupling 2



TITLE: Zynq Decoupling 2
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU102_REV1_0

ASSY P/N: 0431959
PCB P/N: 1280868
SCH P/N: 0381701
TEST P/N: TSS0179

DATE: 09/20/2016:10:35

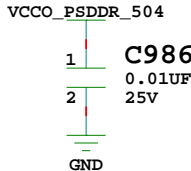
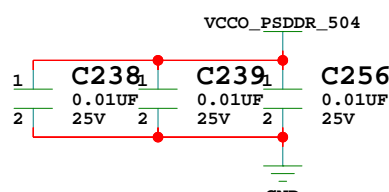
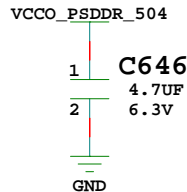
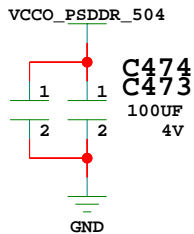
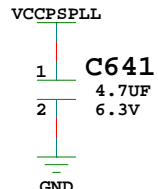
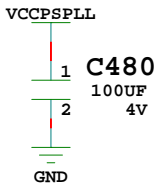
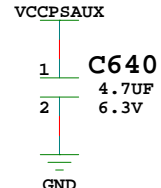
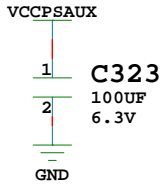
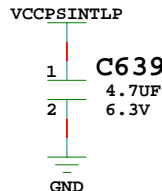
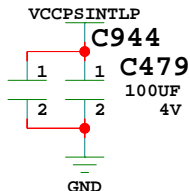
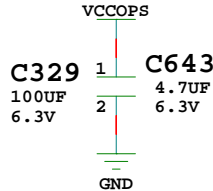
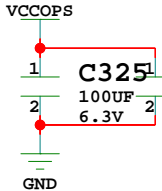
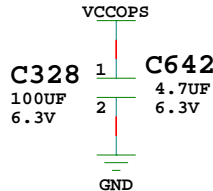
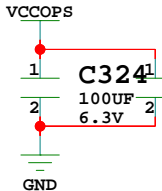
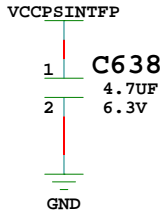
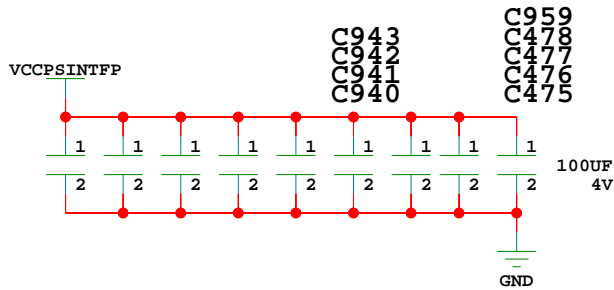
VER:	1.0
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SHEET SIZE: B

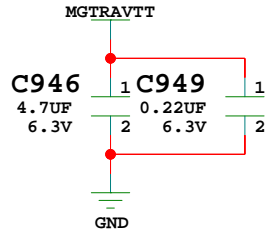
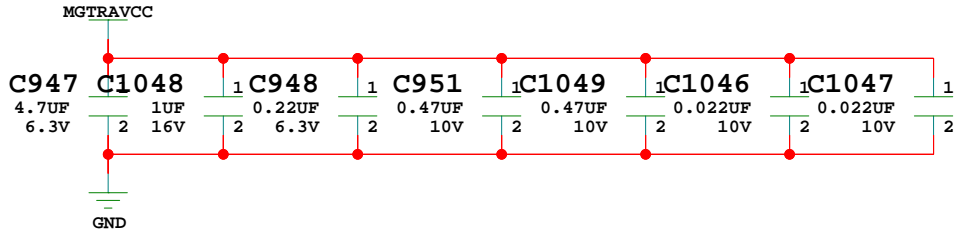
REV:	01
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SHEET 20 OF 87

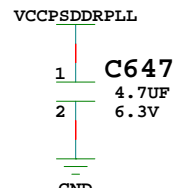
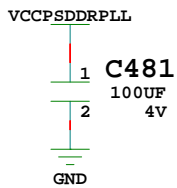
DRAWN BY: BF



BANK 505



Place this round pad
resistor directly under U1



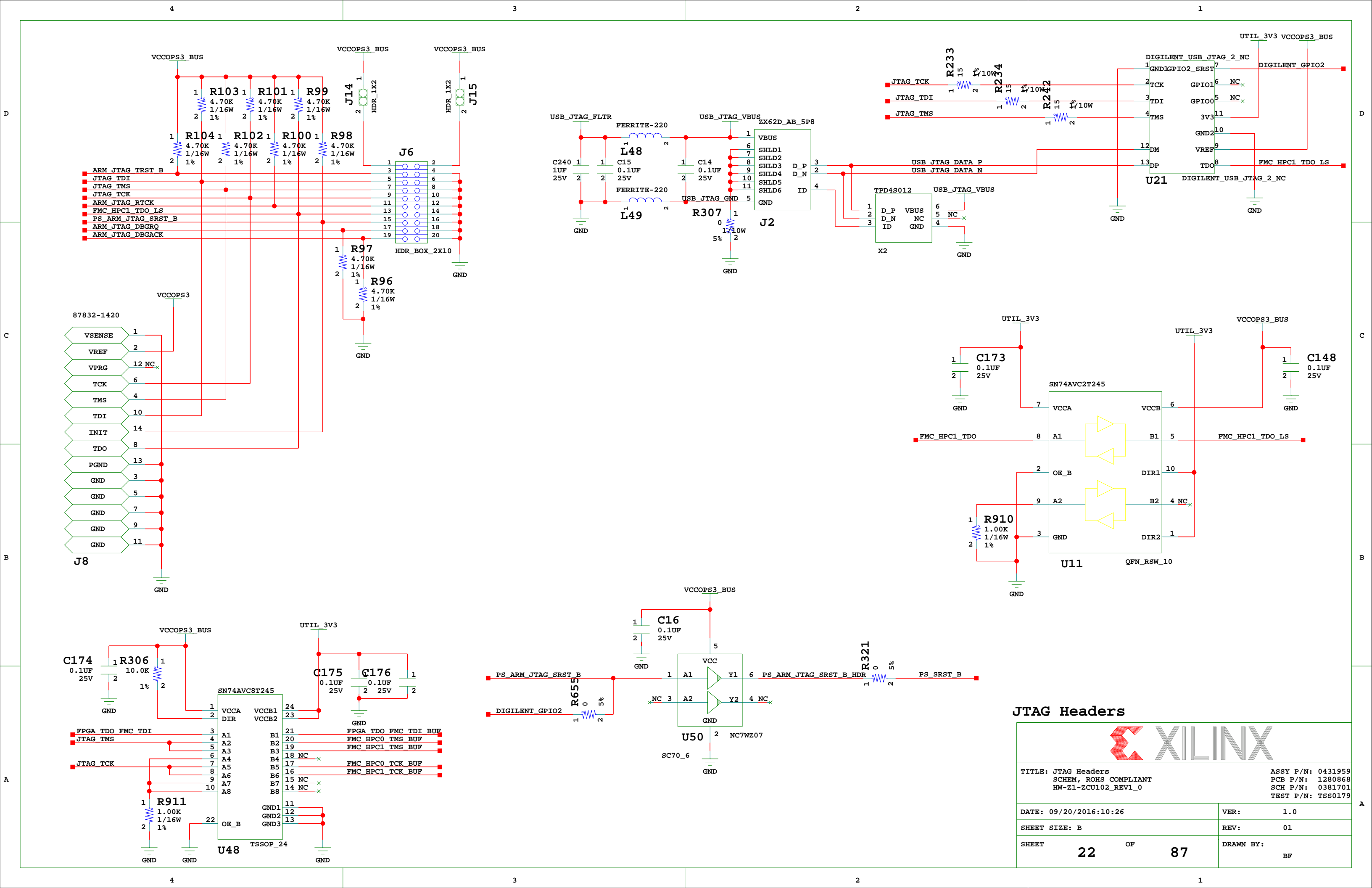
Zynq Decoupling 3



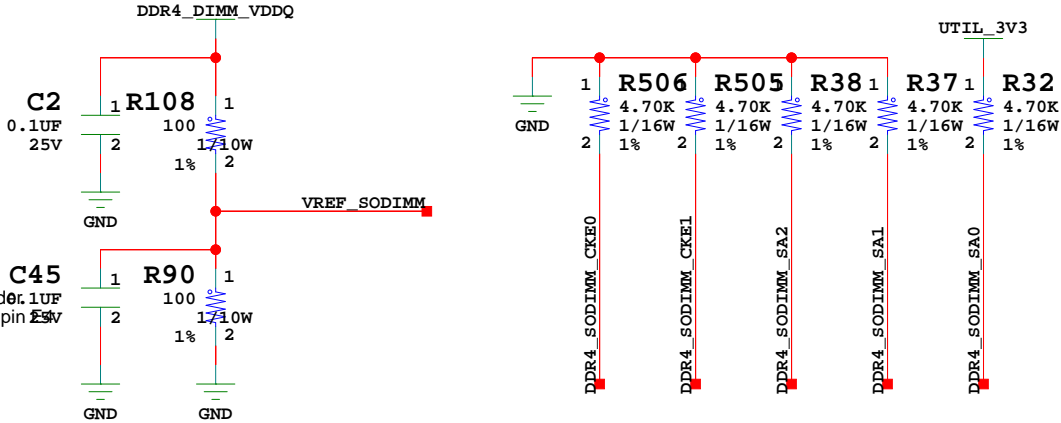
TITLE: Zynq Decoupling 3
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU102_REV1_0

ASSY P/N: 0431959
PCB P/N: 1280868
SCH P/N: 0381701
TEST P/N: TSS0179

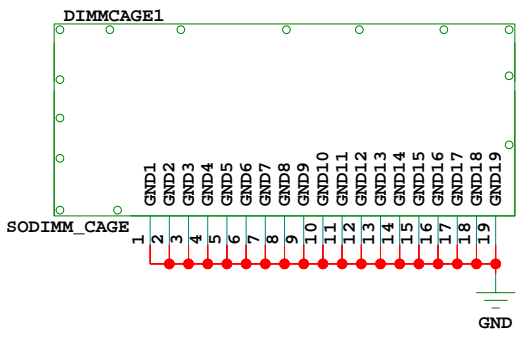
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 21 OF 87	DRAWN BY: BF



Layout Directive:
Place 0.1uF cap under 1uF
memory adjacent to pin 25V

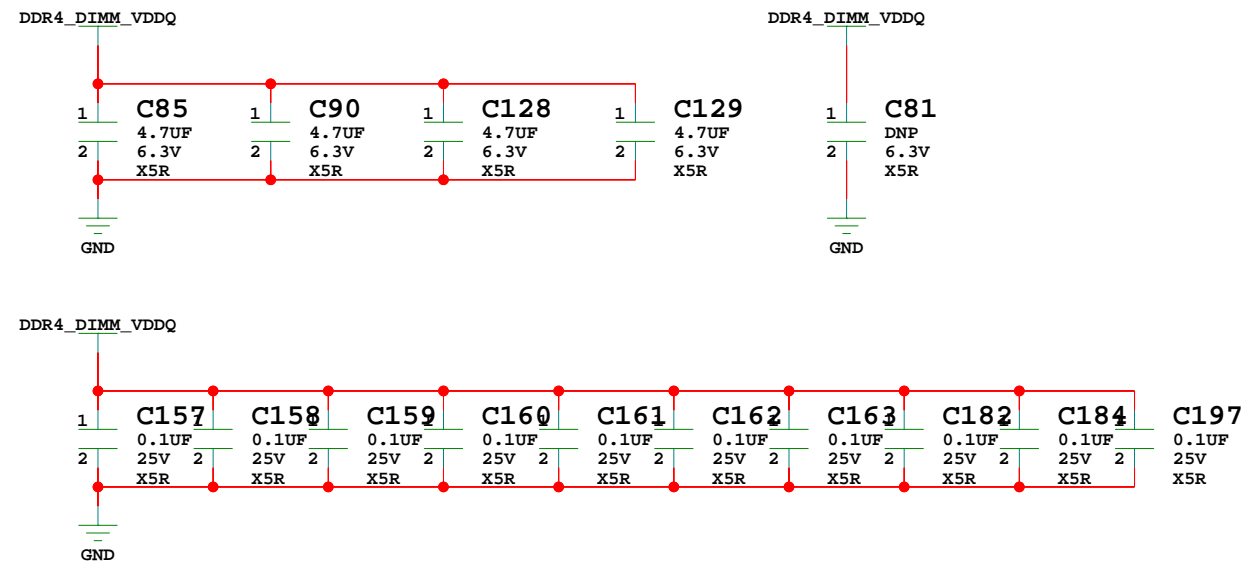


IIC Address = 0b1010001 (0x51)
SODIMM SA[2:0]=001

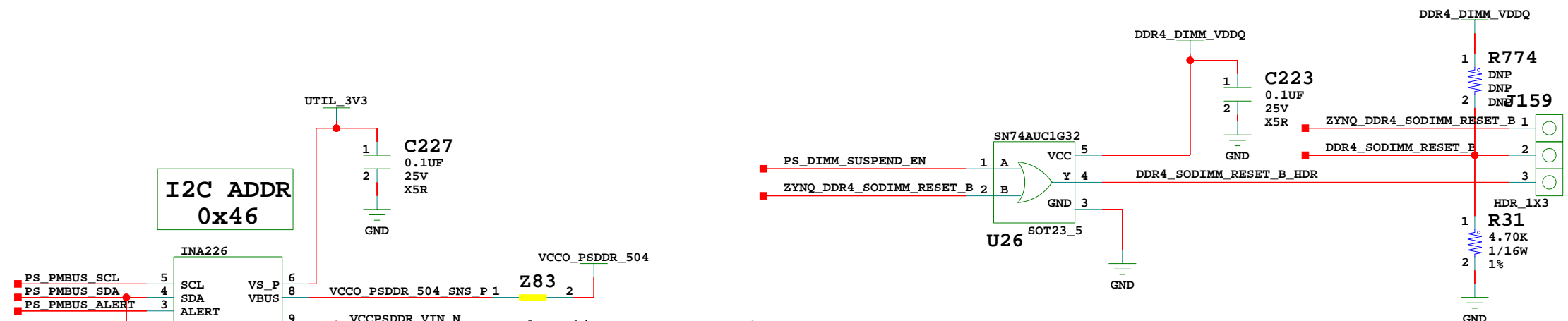


PS DDR4 SODIMM 72 bit

TITLE: PS DDR4 SODIMM 72 bit SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	
ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179	
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 23 OF 87	DRAWN BY: BF

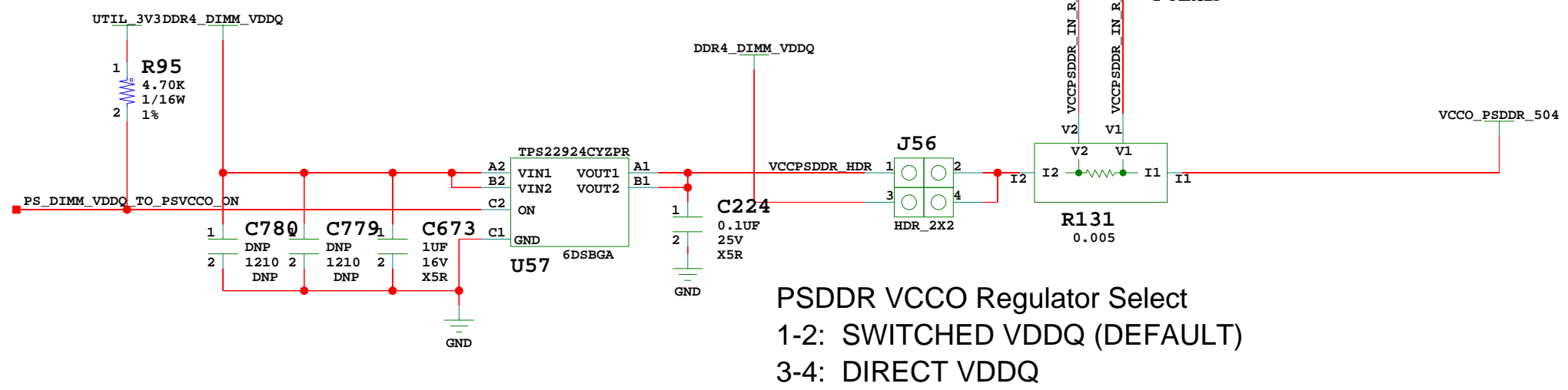


PLACE ABOVE CAPS BENEATH/CLOSE TO DIMM SOCKET



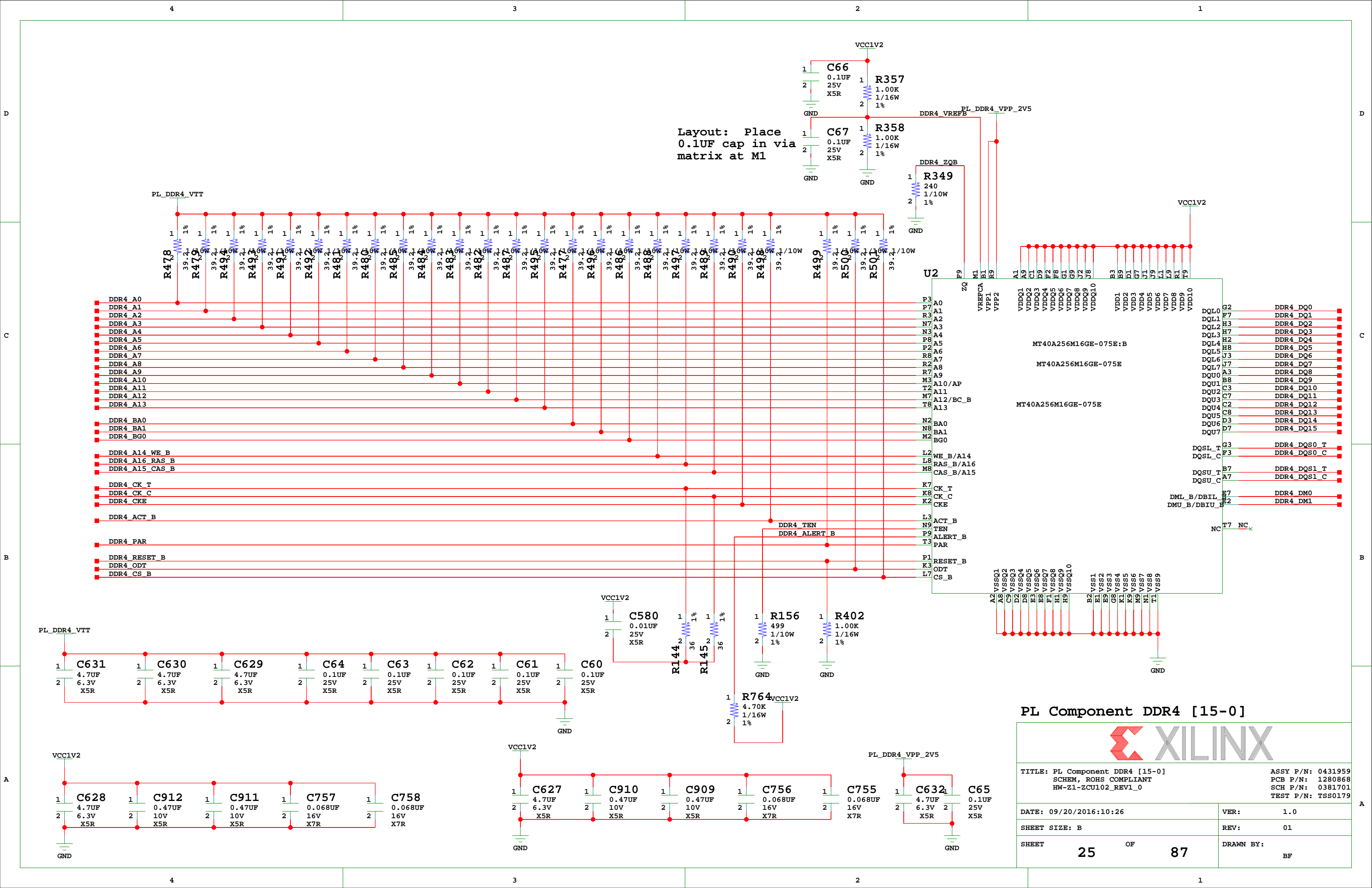
DDR DIMM VCCO DISABLE

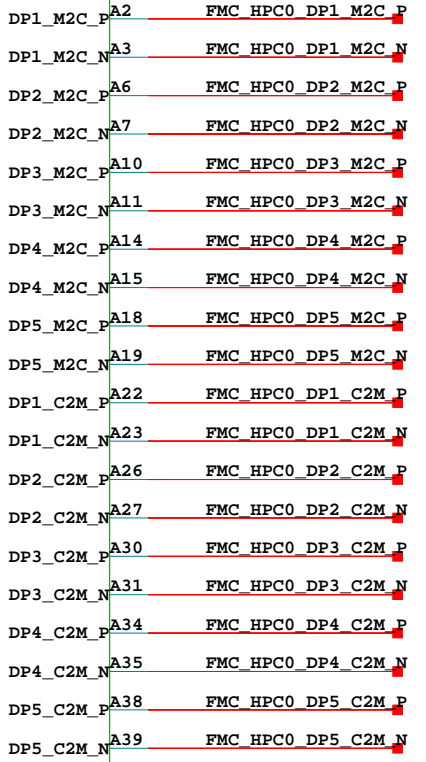
DDR DIMM RESET_B CONTROL



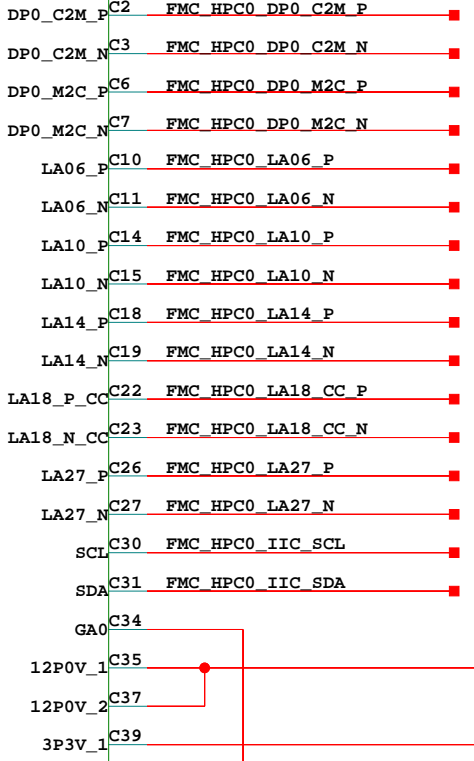
PS DDR4 SODIMM Decoupling

TITLE: PS DDR4 SODIMM Decoupling SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	
ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179	
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 24 OF 87	DRAWN BY: BF

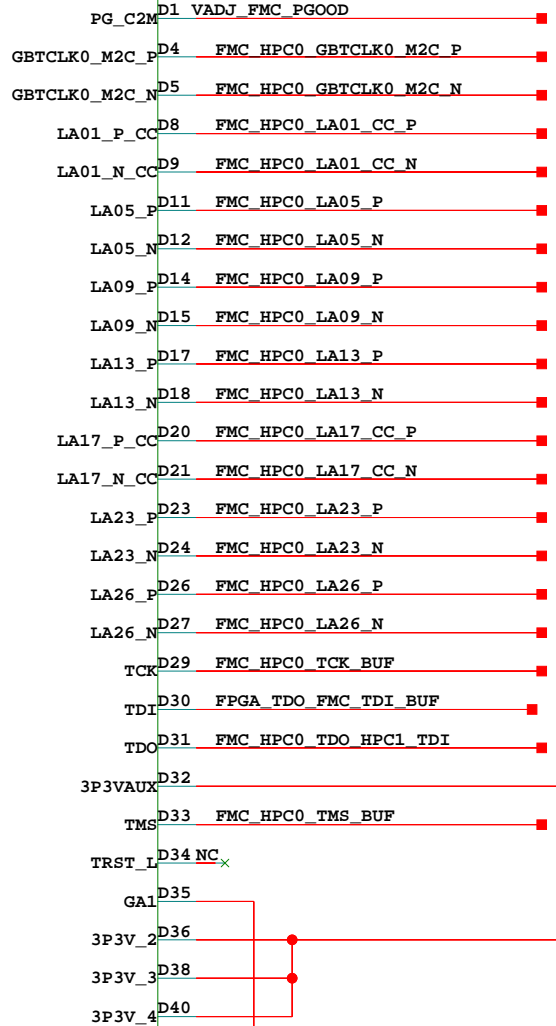




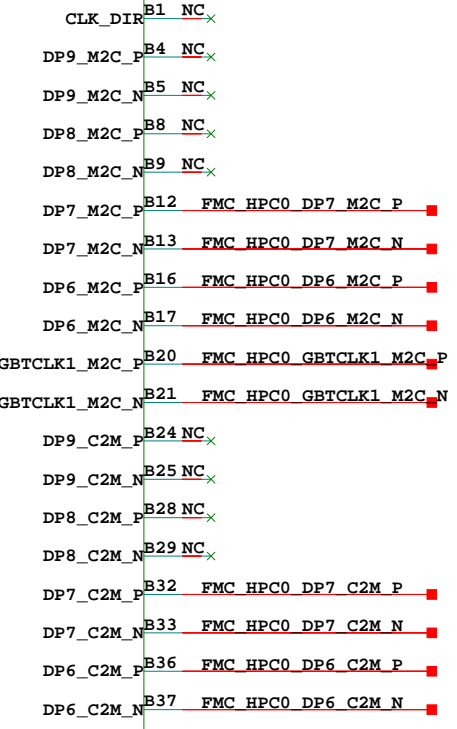
J5 ASP_134486_01



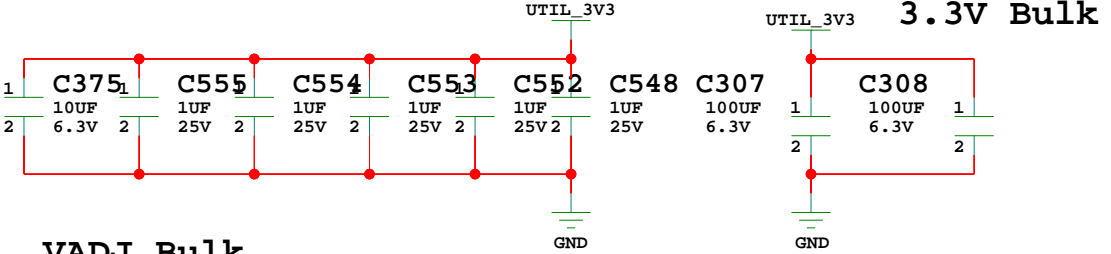
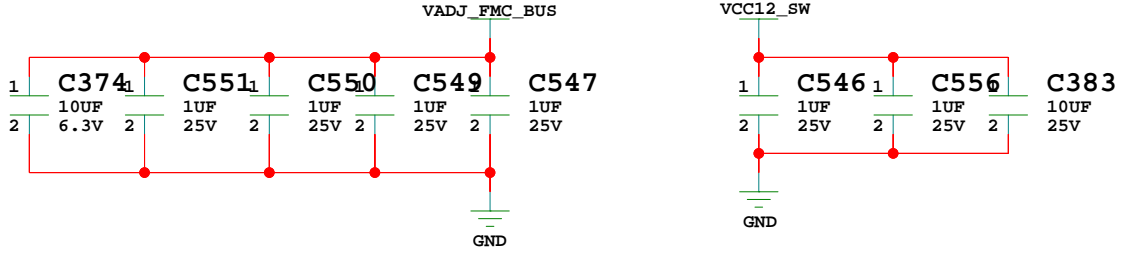
J5 ASP_134486_01



J5 ASP_134486_01

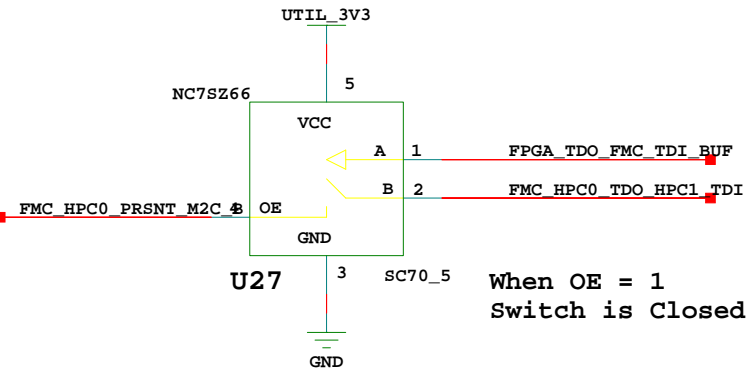
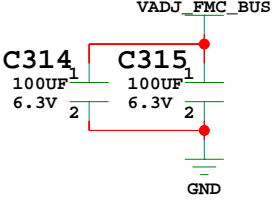


J5 ASP_134486_01



VADJ Bulk

3.3V Bulk



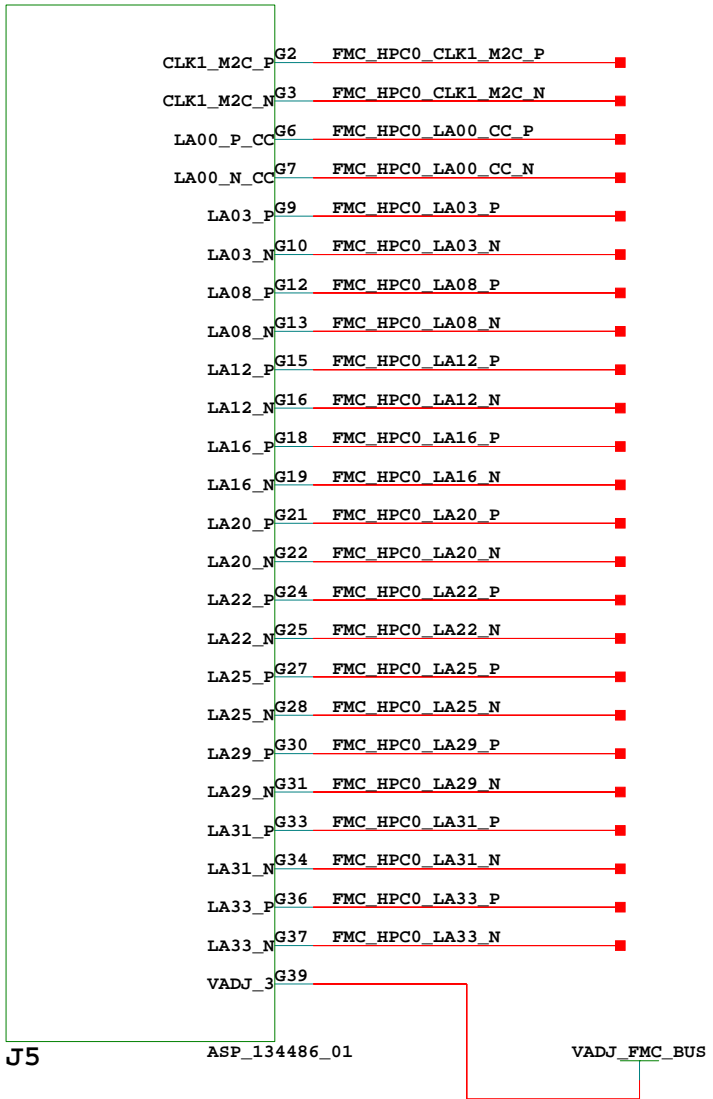
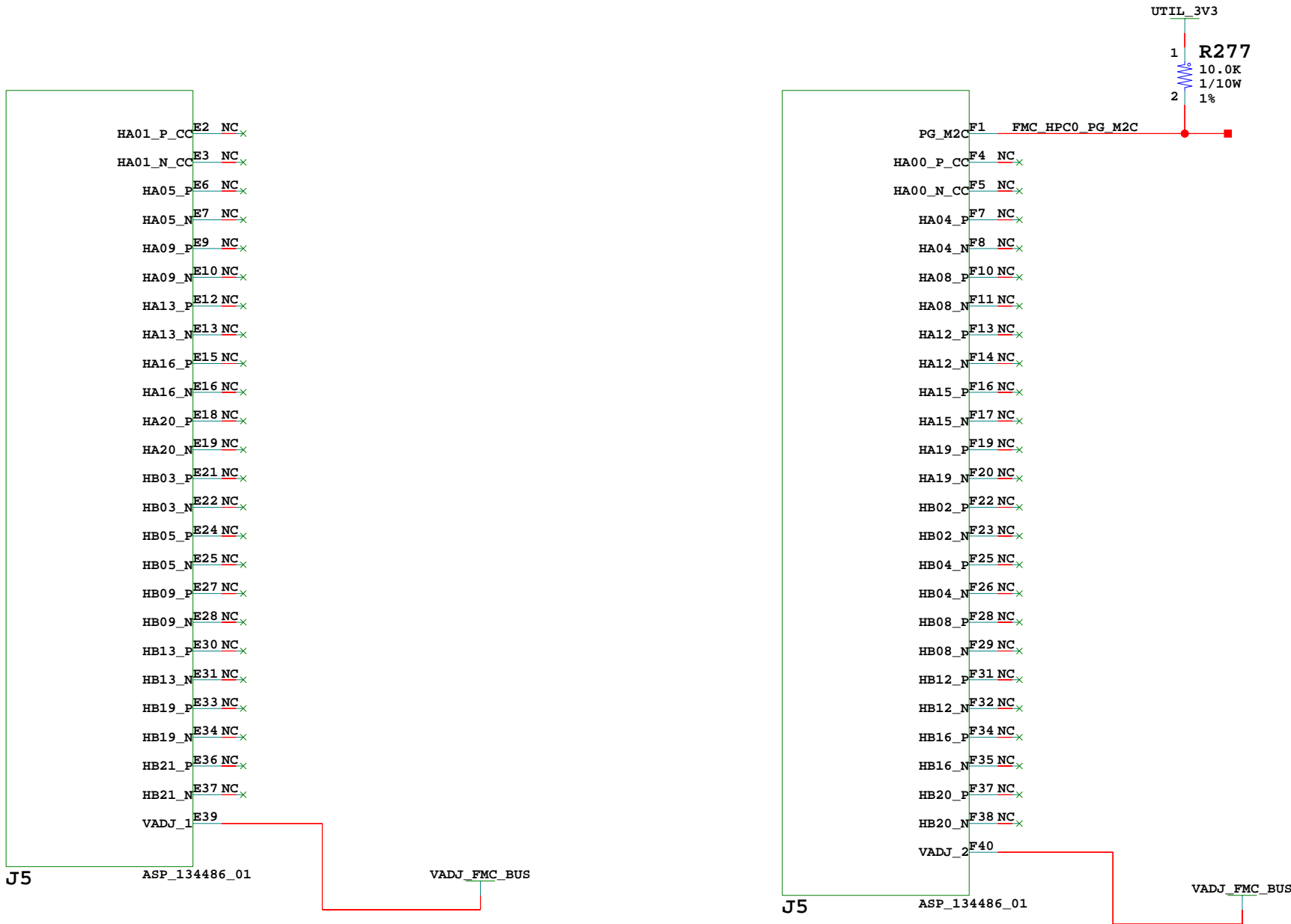
When OE = 1
Switch is Closed

ANSI/VITA 57.1 - Revised 2010
PL FMC HPC0 Header Rows A B C D



TITLE: PL FMC HPC0 Header Rows A B C D
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU102_REV1_0
ASSY P/N: 0431959
PCB P/N: 1280868
SCH P/N: 0381701
TEST P/N: TSS0179

DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 26 OF 87	DRAWN BY: BF



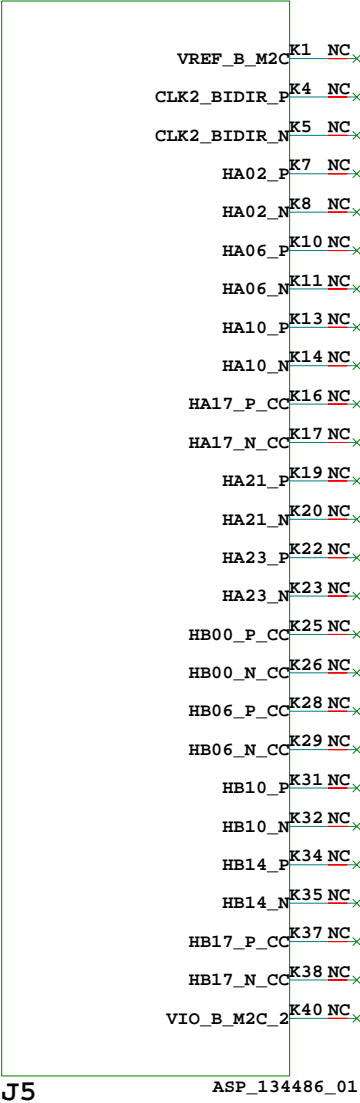
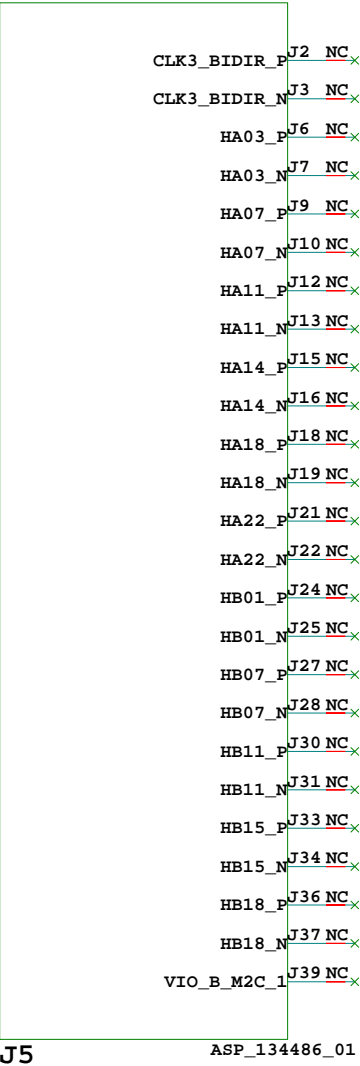
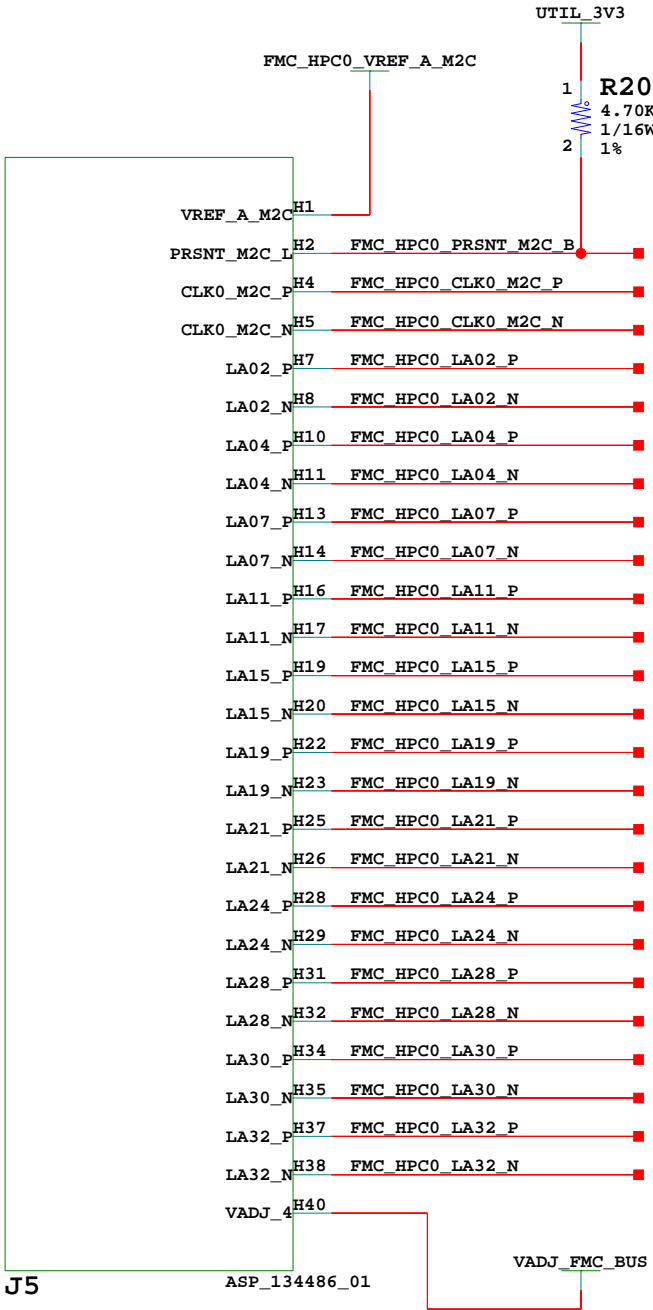
ANSI/VITA 57.1 - Revised 2010
PL FMC HPC0 Header Rows E F G



TITLE: PL FMC HPC0 Header Rows E F G
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU102_REV1_0

ASSY P/N: 0431959
PCB P/N: 1280868
SCH P/N: 0381701
TEST P/N: TSS0179

DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 27 OF 87	DRAWN BY: BF



ANSI/VITA 57.1 - Revised 2010
PL FMC HPC0 Header Rows H J K

TITLE: PL FMC HPC0 Header Rows H J K SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0		ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179	
DATE: 09/20/2016:10:26		VER:	1.0
SHEET SIZE: B		REV:	01
SHEET	28	OF	87
		DRAWN BY:	BF



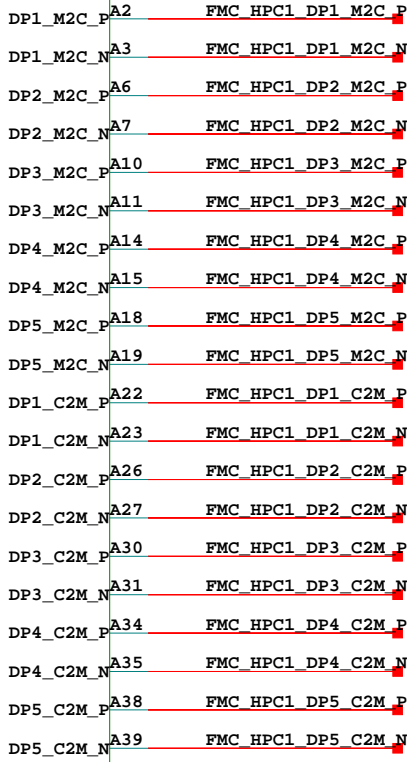
ANSI/VITA 57.1 - Revised 2010
PL FMC HPC0 Header GND



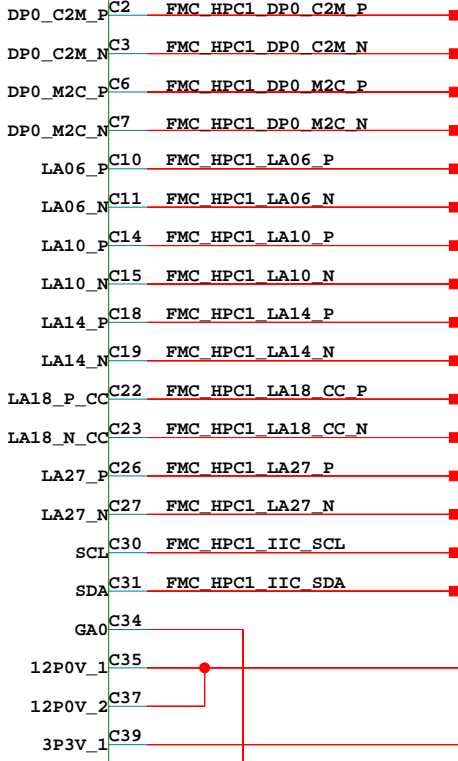
TITLE: PL FMC HPC0 Header GND
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU102_REV1_0

ASSY P/N: 0431959
PCB P/N: 1280868
SCH P/N: 0381701
TEST P/N: TSS0179

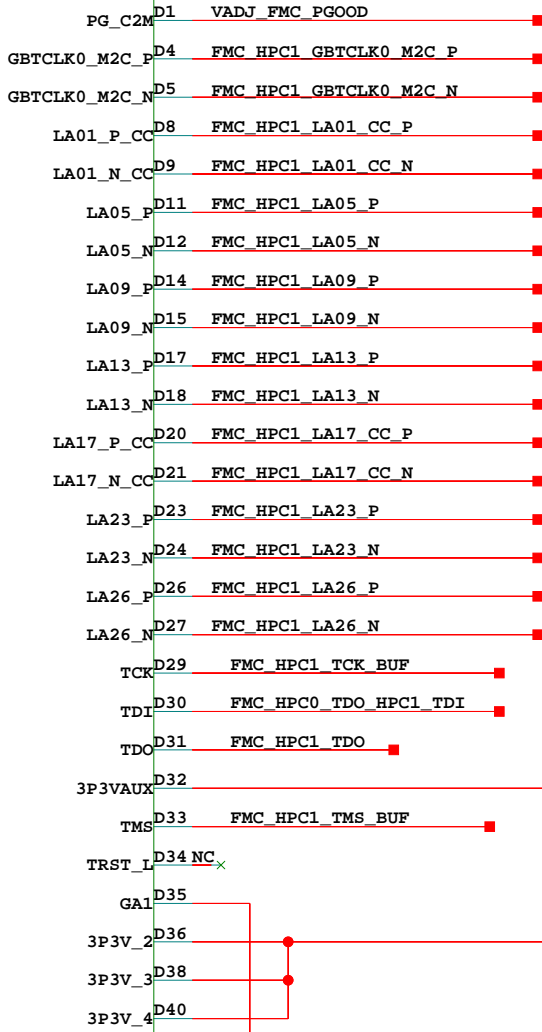
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 29 OF 87	DRAWN BY: BF



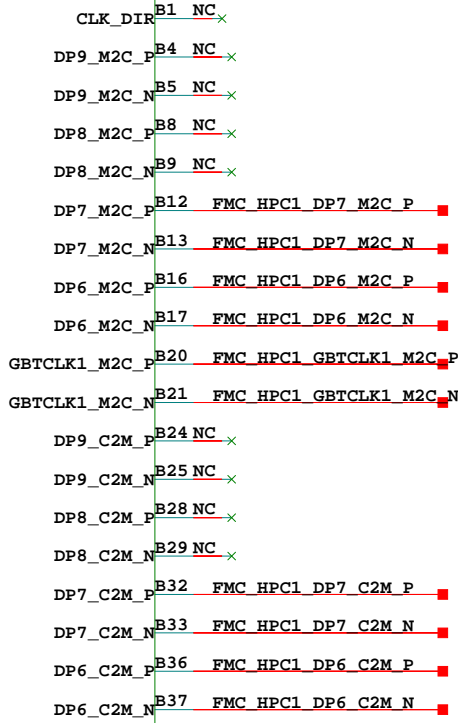
J4 ASP_134486_01



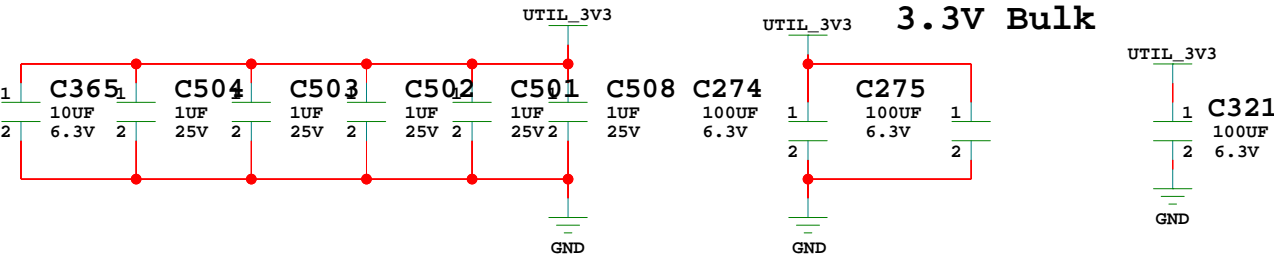
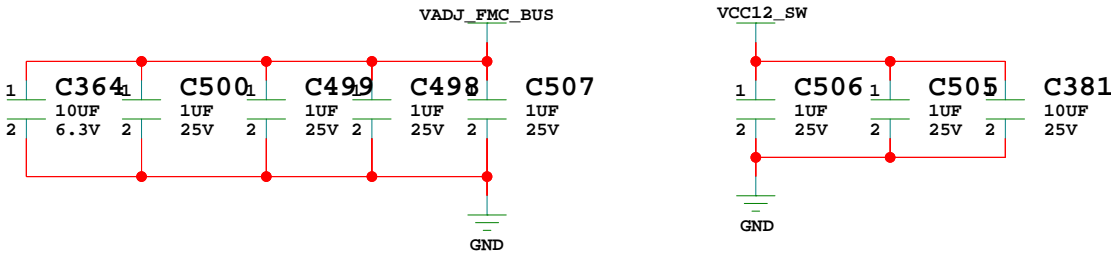
J4 ASP_134486_01



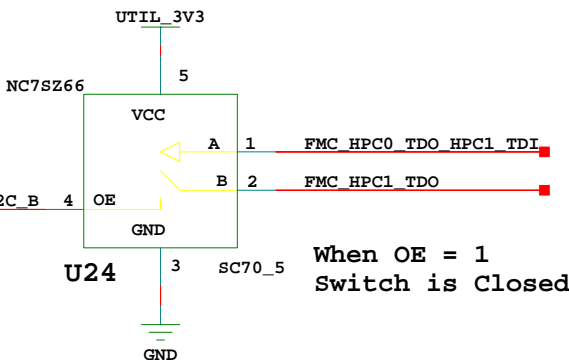
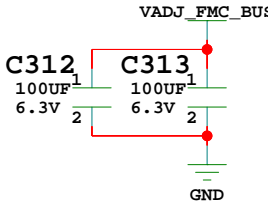
J4 ASP_134486_01



J4 ASP_134486_01



VADJ Bulk

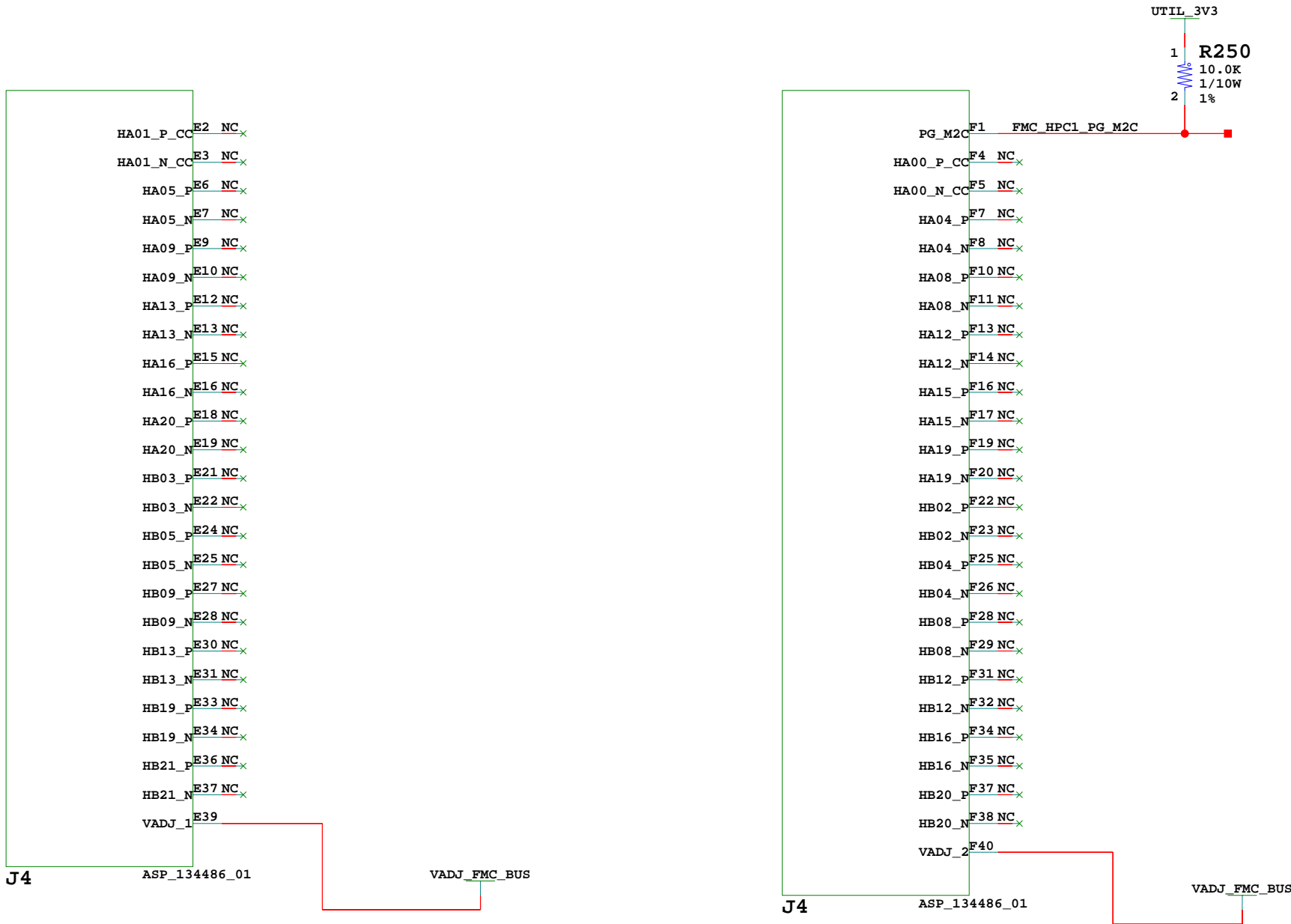


ANSI/VITA 57.1 - Revised 2010
PL FMC HPC1 Header Rows A B C D



TITLE: PL FMC HPC1 Header Rows A B C D
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU102_REV1_0
ASSY P/N: 0431959
PCB P/N: 1280868
SCH P/N: 0381701
TEST P/N: TSS0179

DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 30 OF 87	DRAWN BY: BF

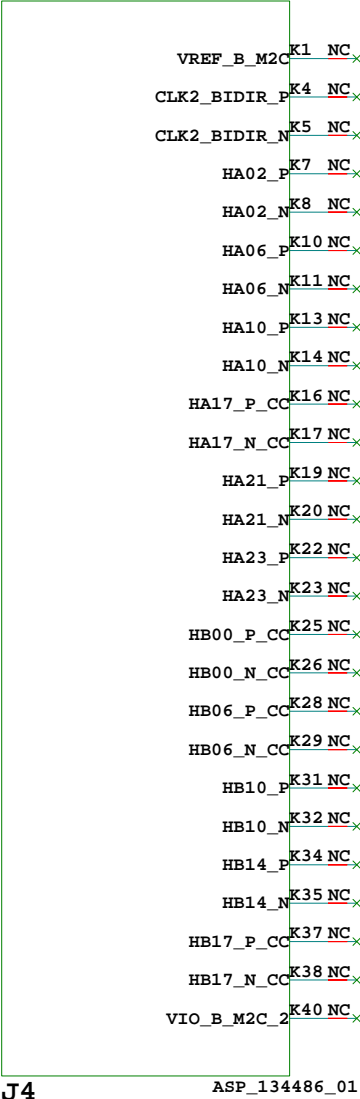
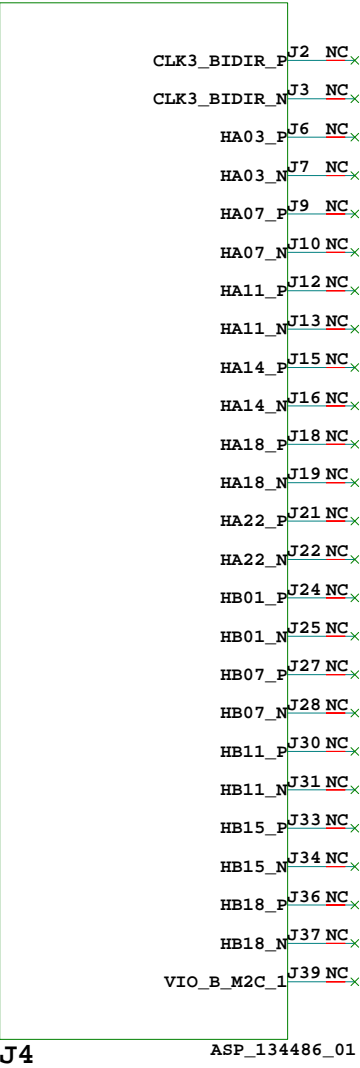
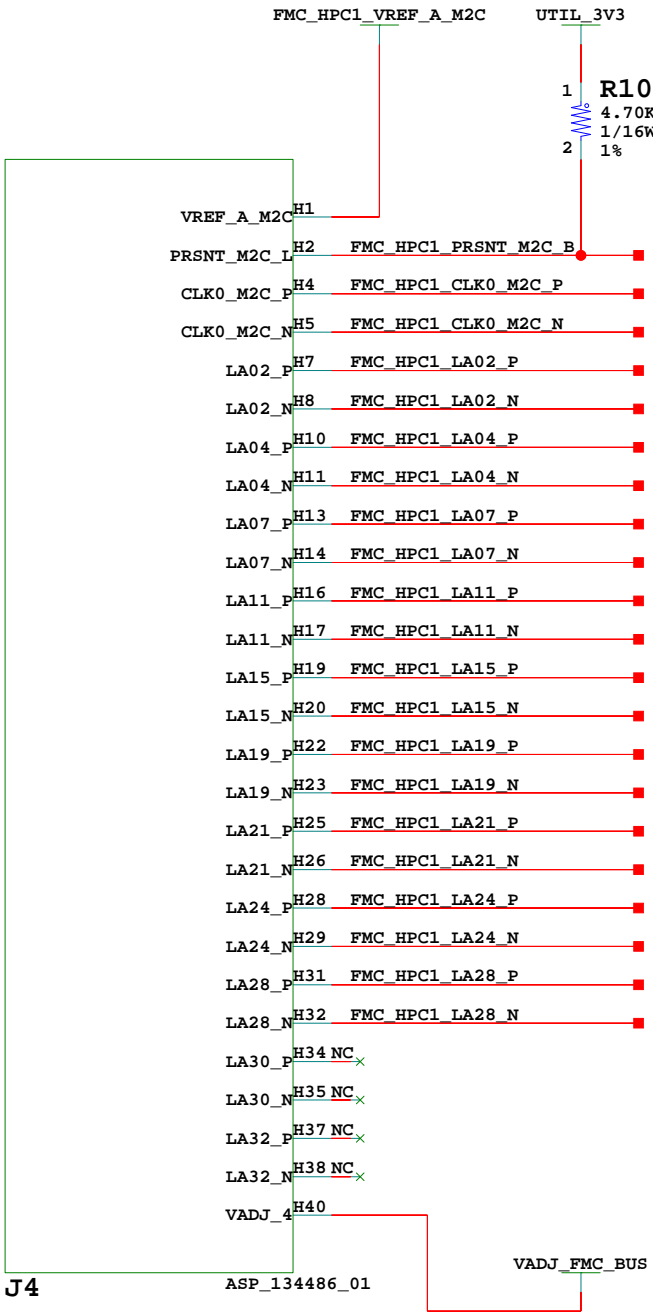


ANSI/VITA 57.1 - Revised 2010
PL FMC HPC1 Header Rows E F G



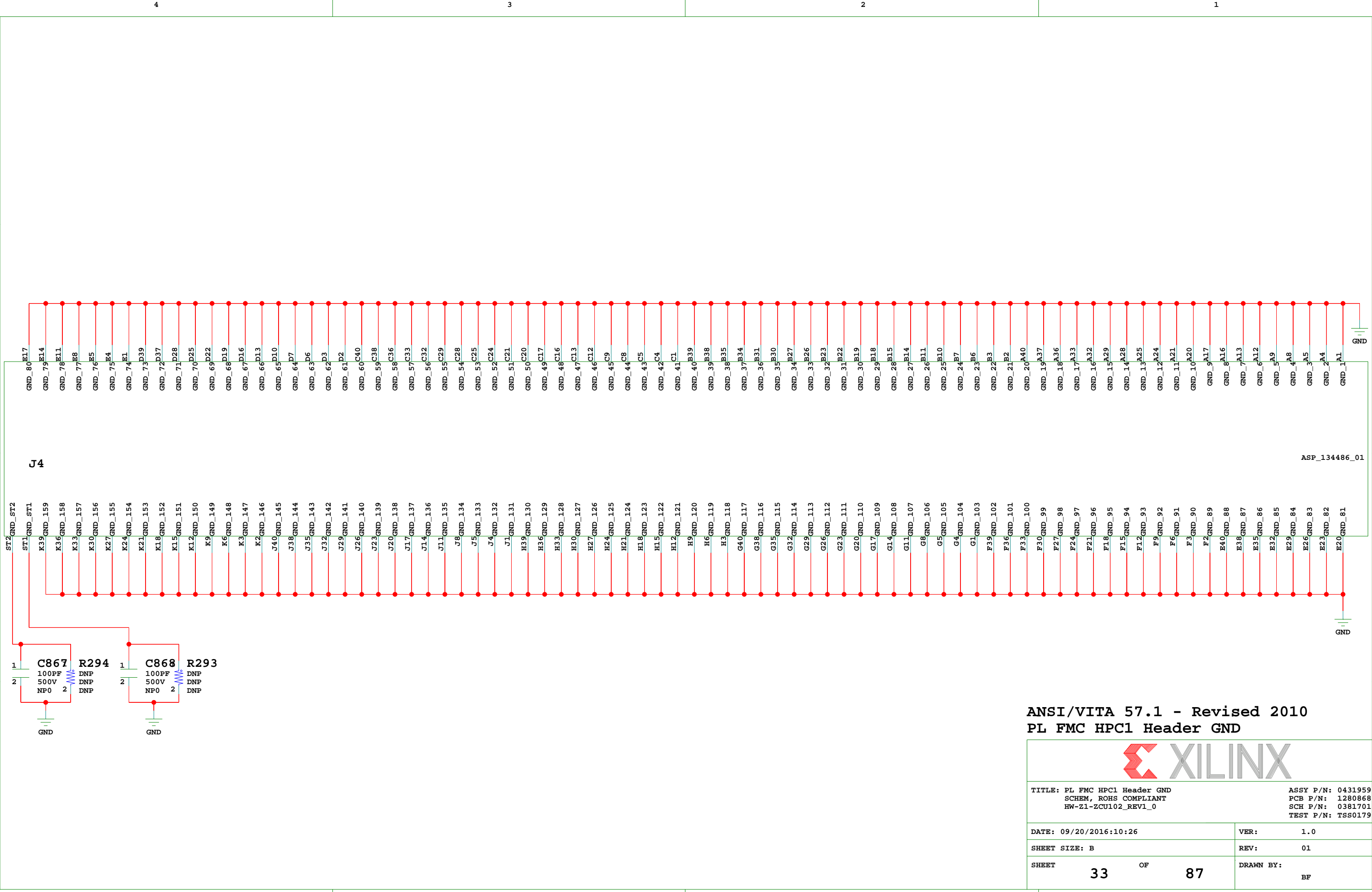
TITLE: PL FMC HPC1 Header Rows E F G
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU102_REV1_0
ASSY P/N: 0431959
PCB P/N: 1280868
SCH P/N: 0381701
TEST P/N: TSS0179

DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 31 OF 87	DRAWN BY: BF



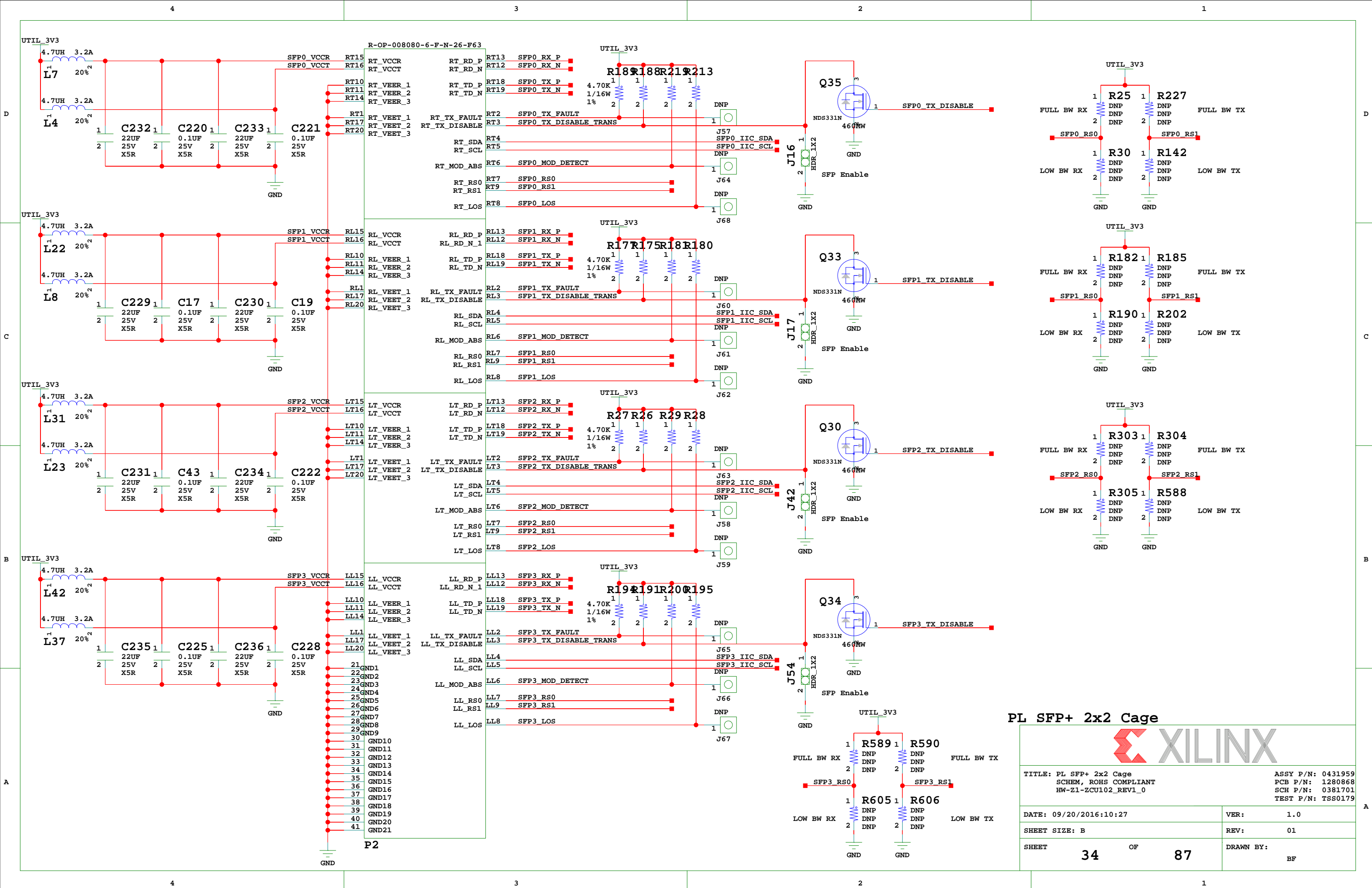
ANSI/VITA 57.1 - Revised 2010
PL FMC HPC1 Header Rows H J K

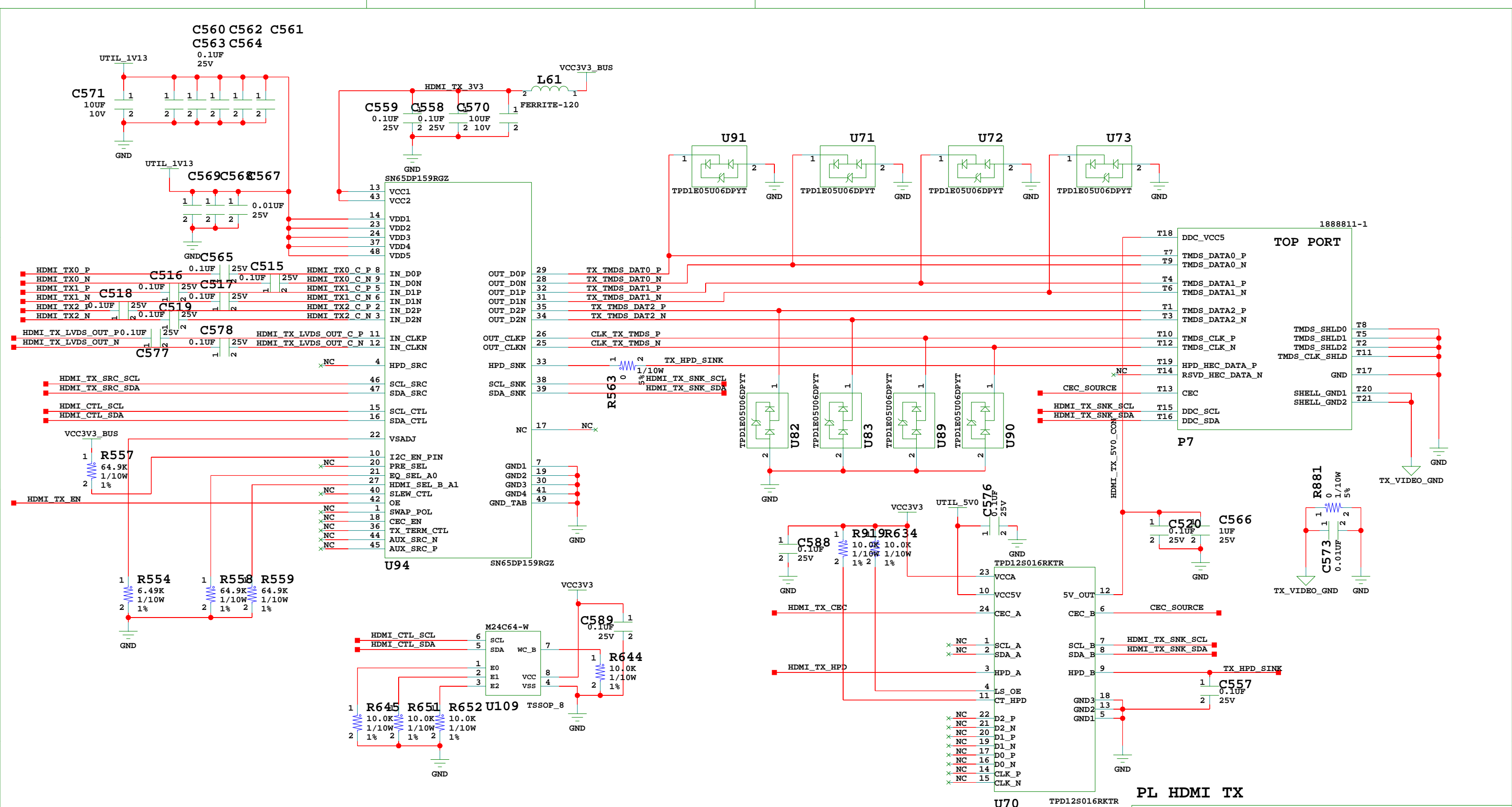
TITLE: PL FMC HPC1 Header Rows H J K SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	
ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179	
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 32 OF 87	DRAWN BY: BF



ANSI/VITA 57.1 - Revised 2010
PL FMC HPC1 Header GND

TITLE: PL FMC HPC1 Header GND SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	
ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179	
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 33 OF 87	DRAWN BY: BF

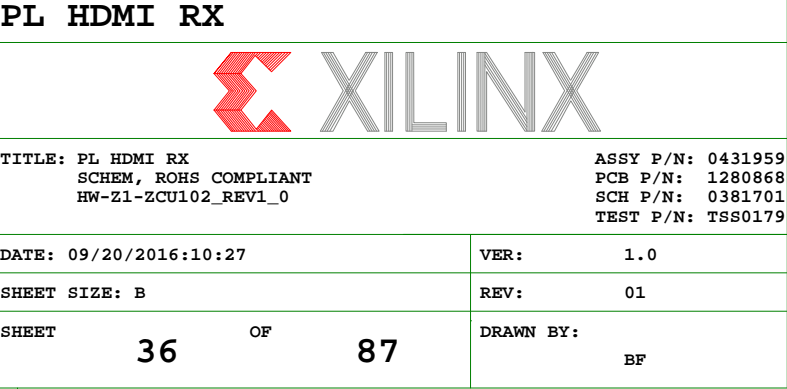


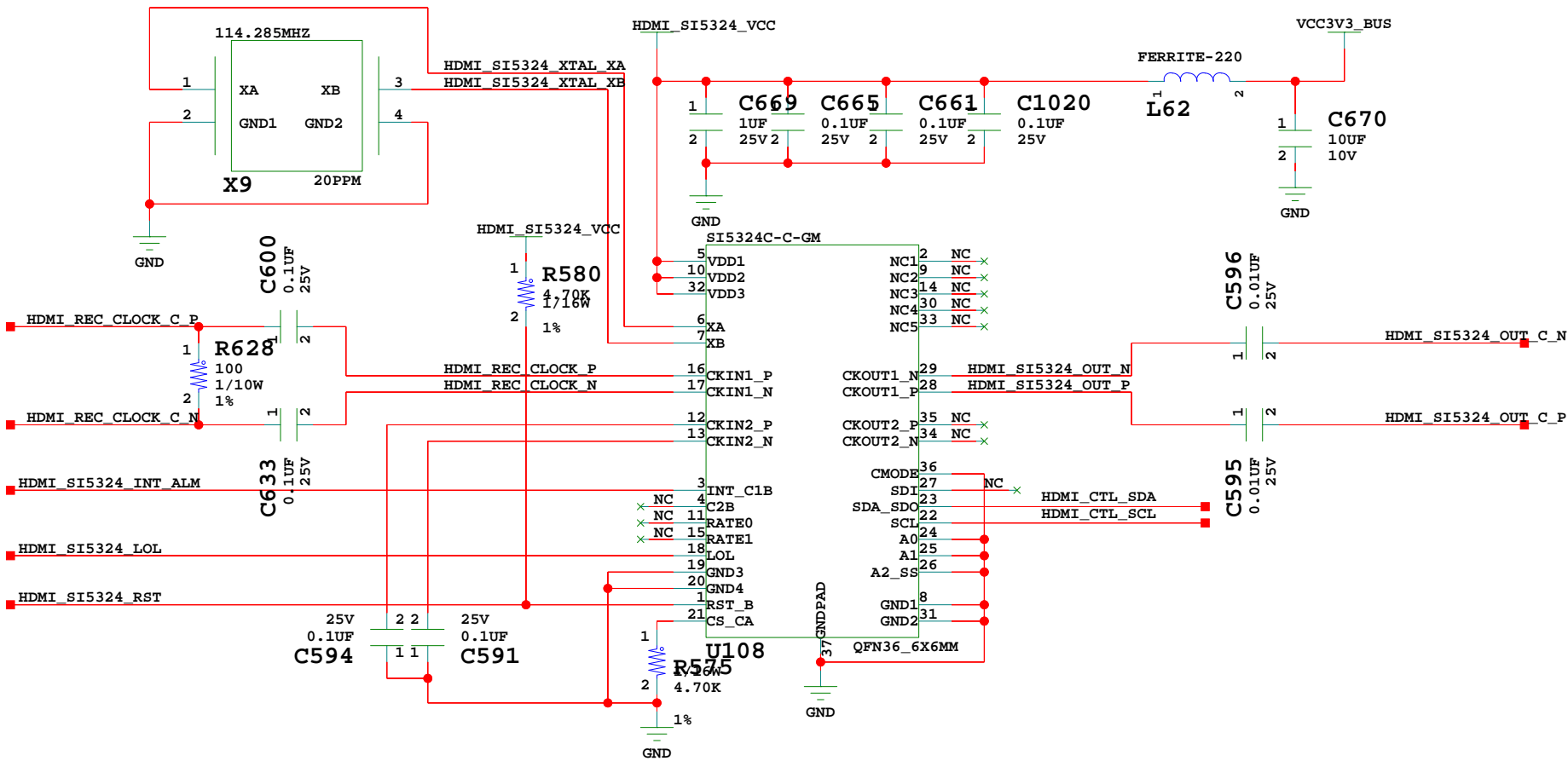


TITLE: PL HDMI TX
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU102_REV1_0

ASSY P/N: 0431959
PCB P/N: 1280868
SCH P/N: 0381701
TEST P/N: TSS0179

DATE: 09/20/2016:10:27	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 35 OF 87	DRAWN BY: BF



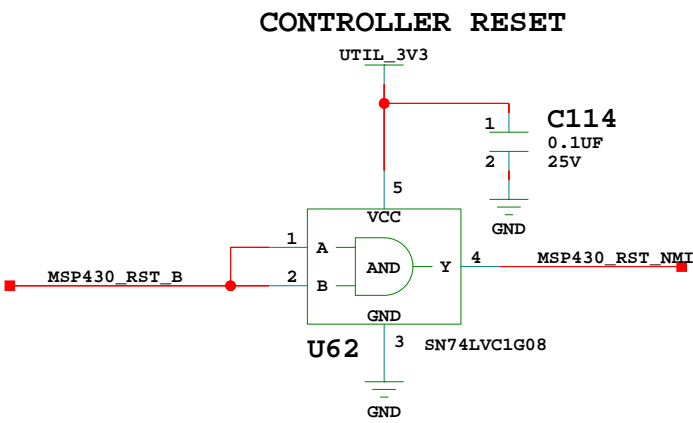
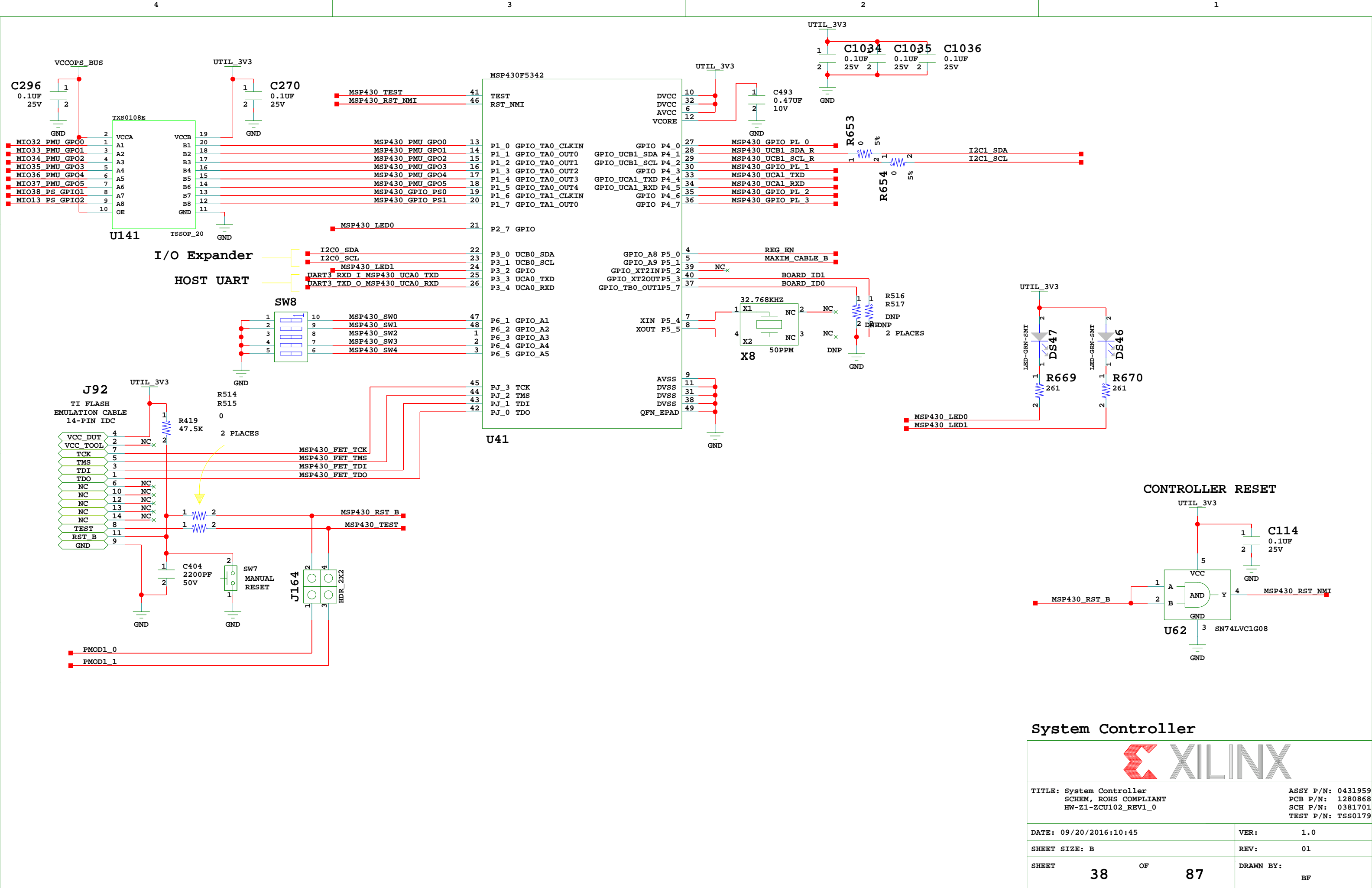


PL HDMI Clock Recovery



TITLE: PL HDMI Clock Recovery SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
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DATE: 09/20/2016:10:27	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 37 OF 87	DRAWN BY: BF



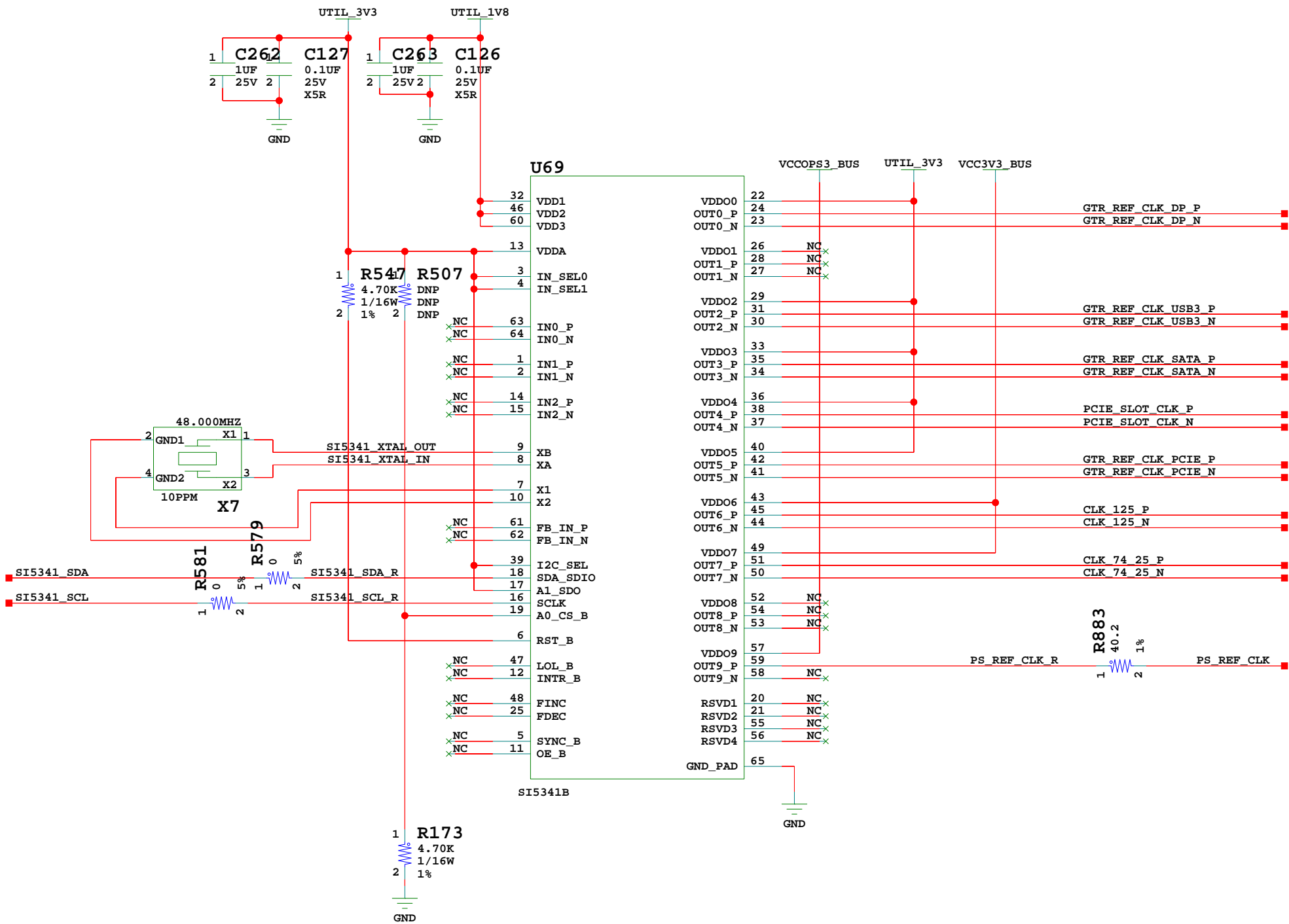
System Controller



TITLE: System Controller
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU102_REV1_0

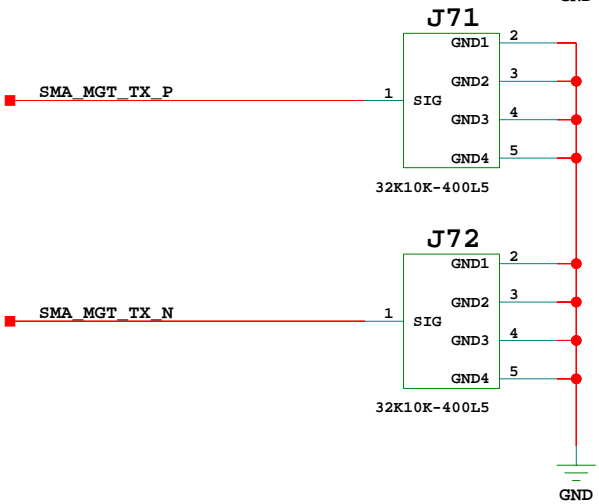
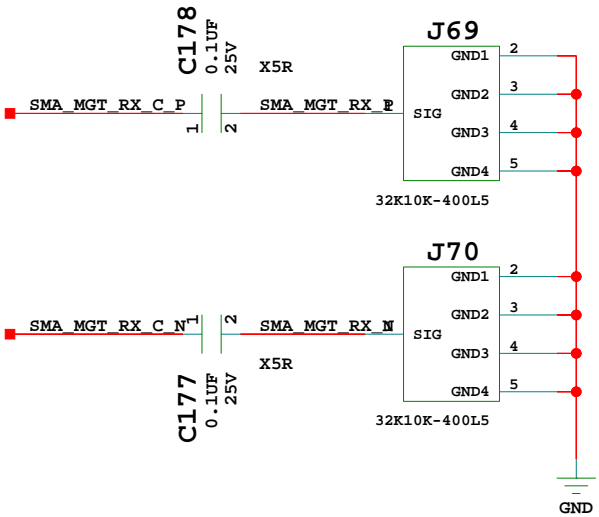
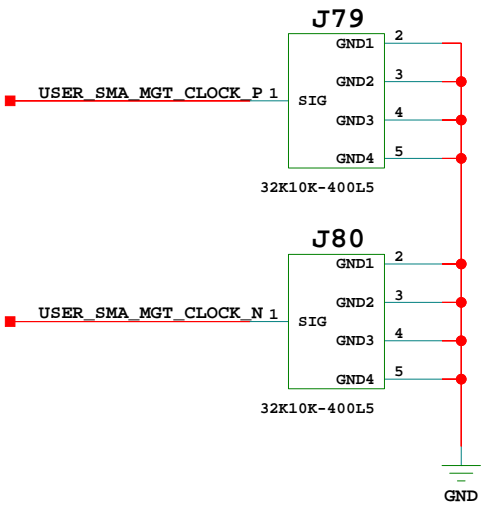
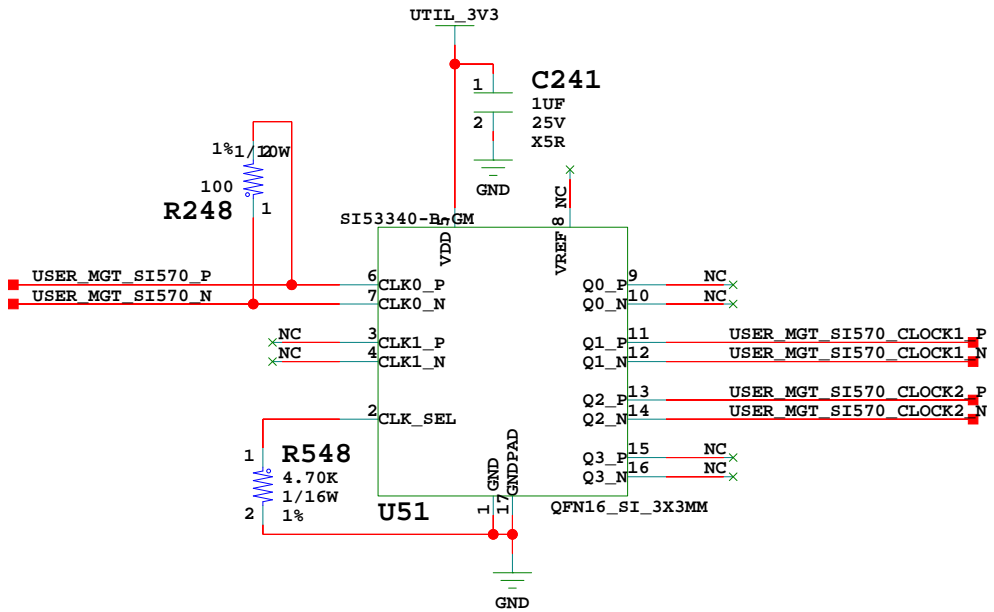
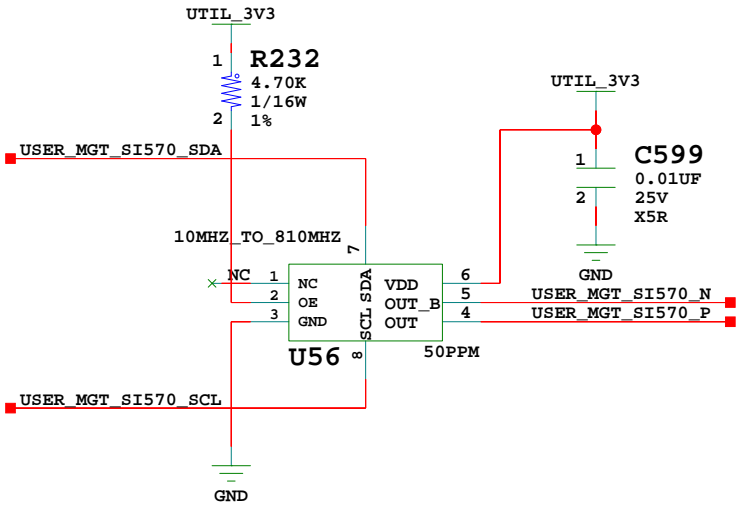
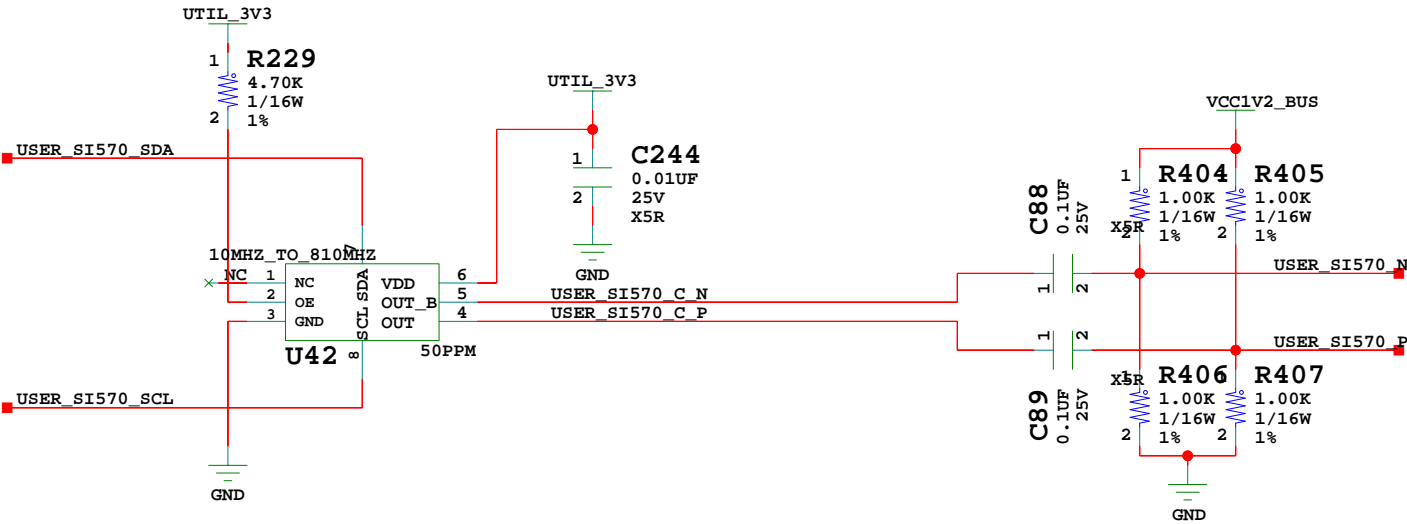
ASSY P/N: 0431959
PCB P/N: 1280868
SCH P/N: 0381701
TEST P/N: TSS0179

DATE: 09/20/2016:10:45	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 38 OF 87	DRAWN BY: BF



Fixed Clocks

TITLE: Fixed Clocks SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	
ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179	
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 39 OF 87	DRAWN BY: BF



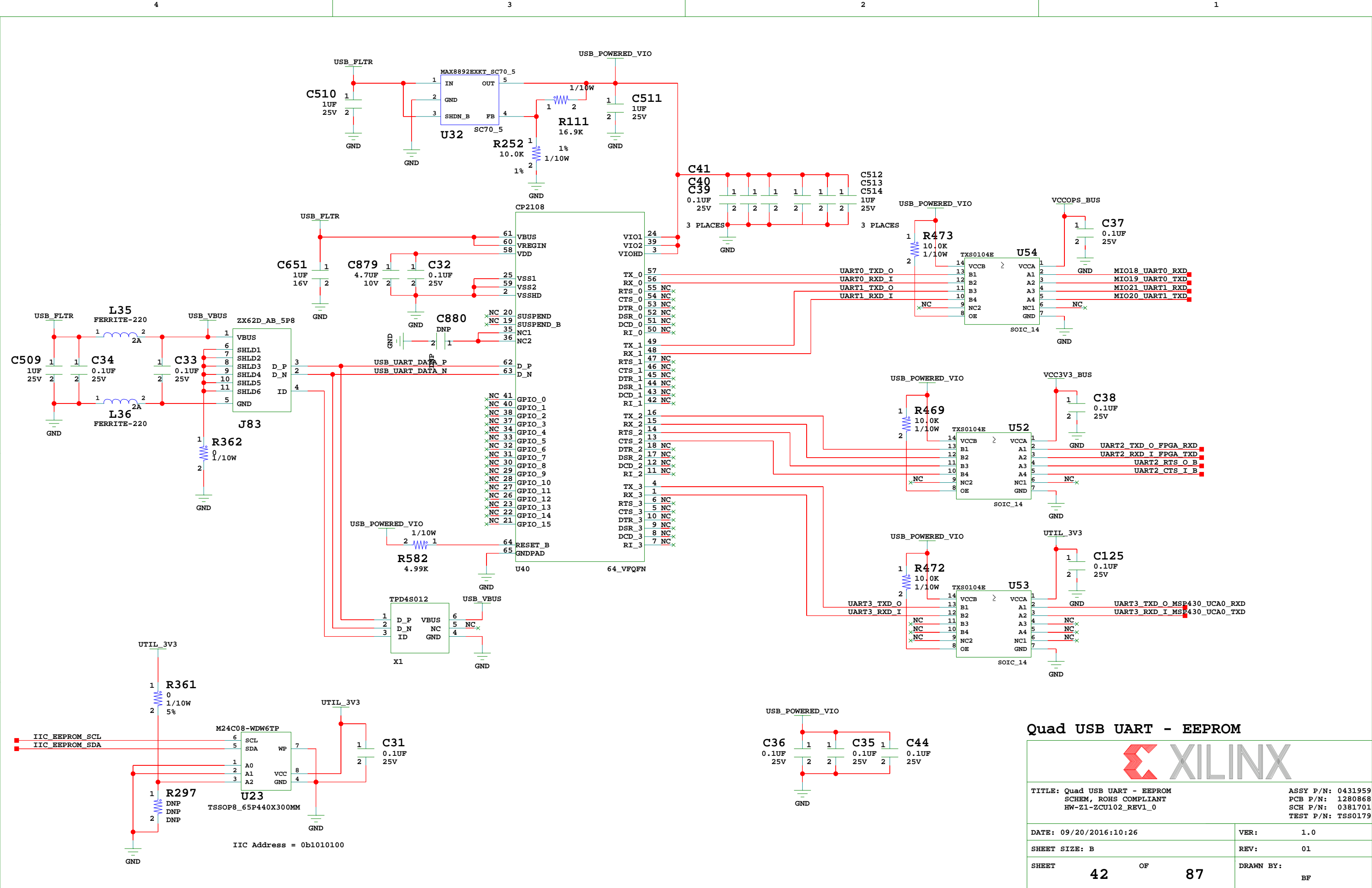
PL Programmable Clocks - SMAs



TITLE: PL Programmable Clocks - SMAs
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU102_REV1_0

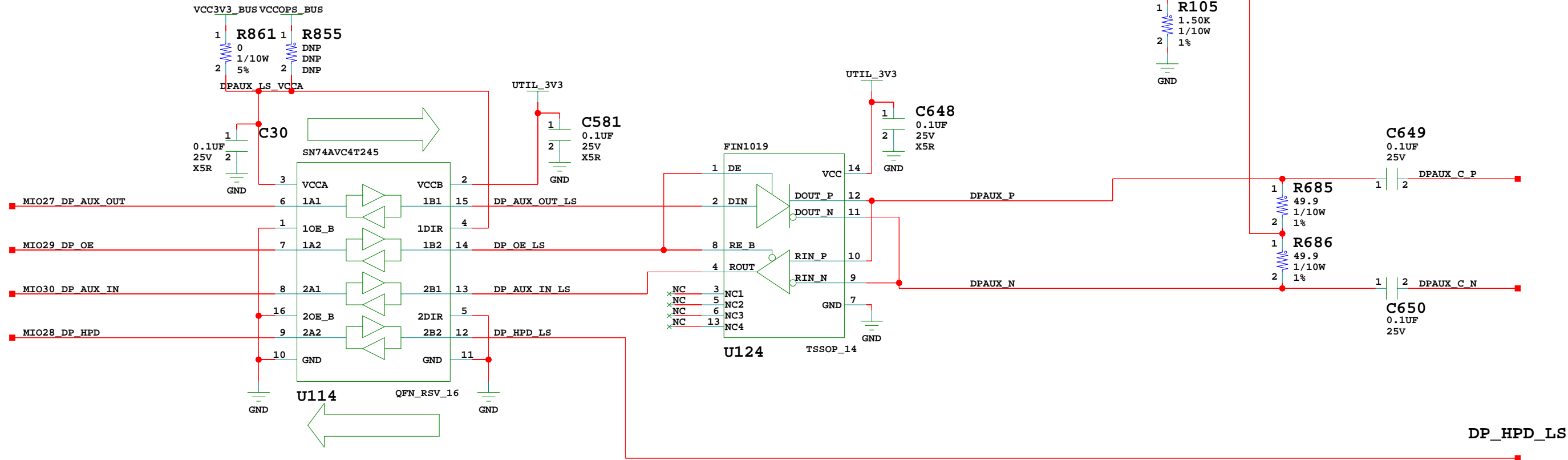
ASSY P/N: 0431959
PCB P/N: 1280868
SCH P/N: 0381701
TEST P/N: TSS0179

DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 40 OF 87	DRAWN BY: BF



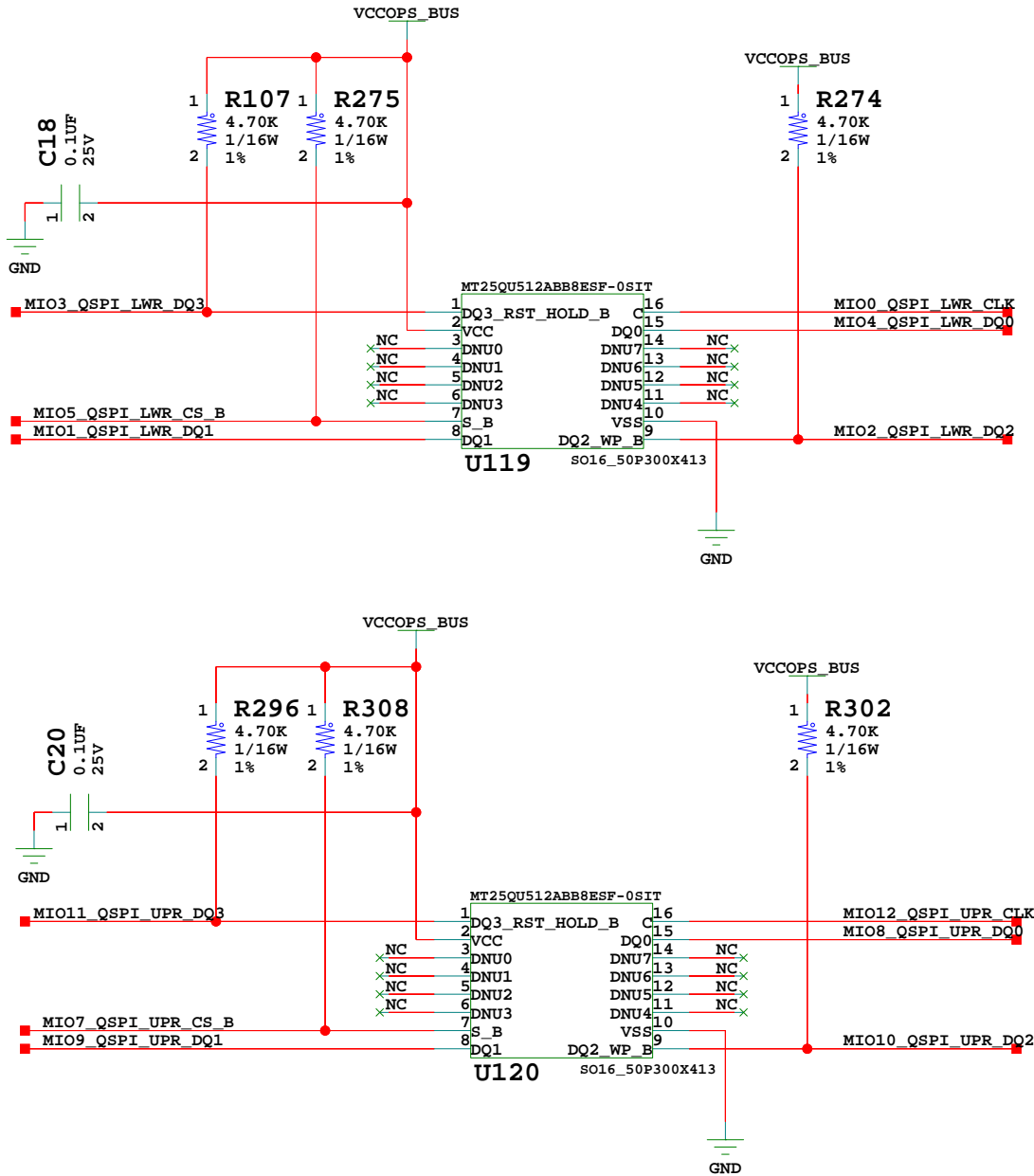
Quad USB UART - EEPROM

TITLE: Quad USB UART - EEPROM SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	
ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179	
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 42 OF 87	DRAWN BY: BF




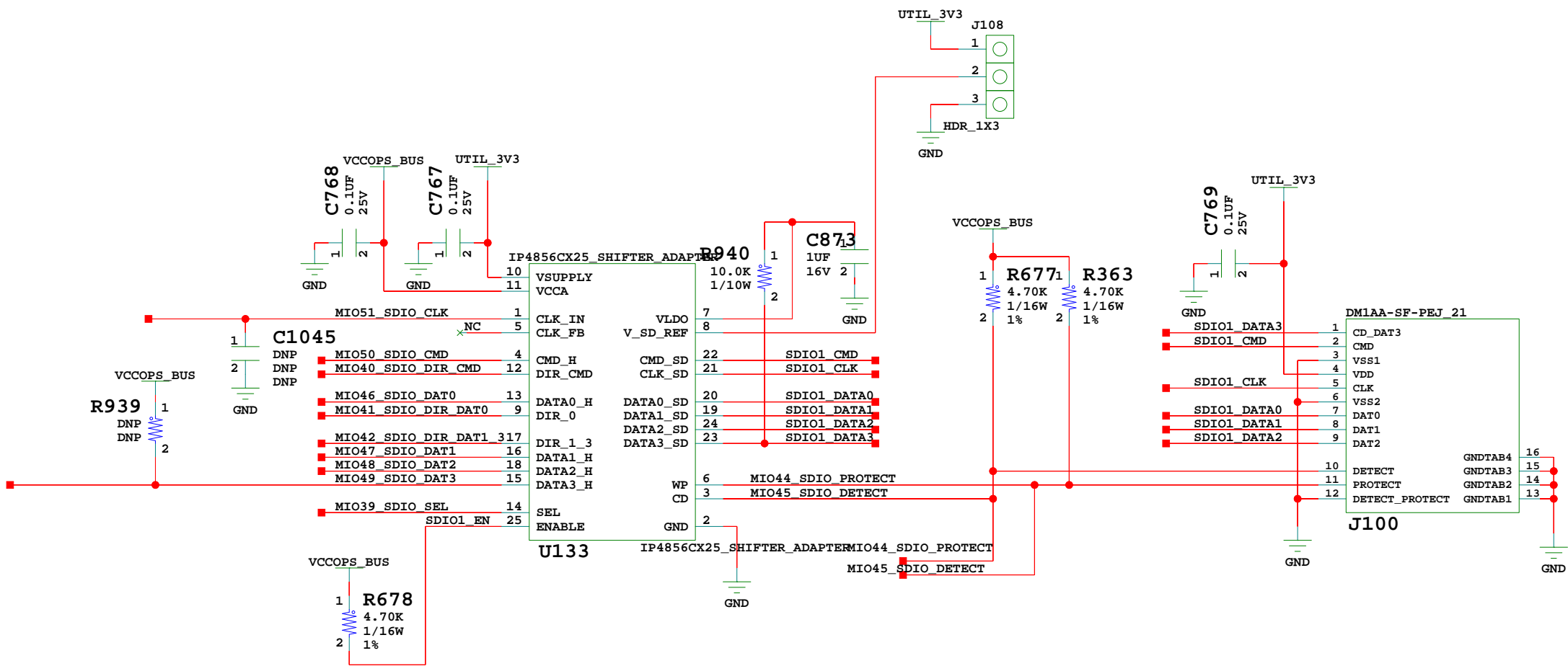
PS Display Port IO

TITLE: PS Display Port IO SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0		ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179	
DATE: 09/20/2016:10:27		VER:	1.0
SHEET SIZE: B		REV:	01
SHEET	45	OF	87
		DRAWN BY:	BF




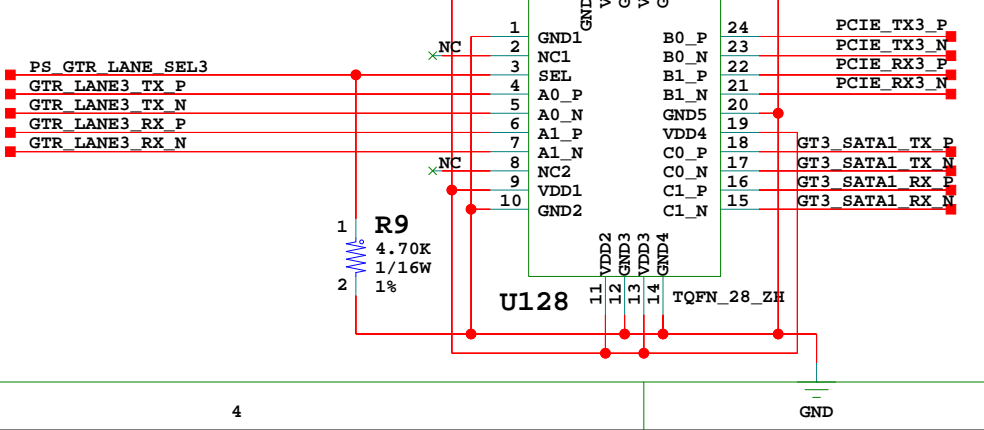
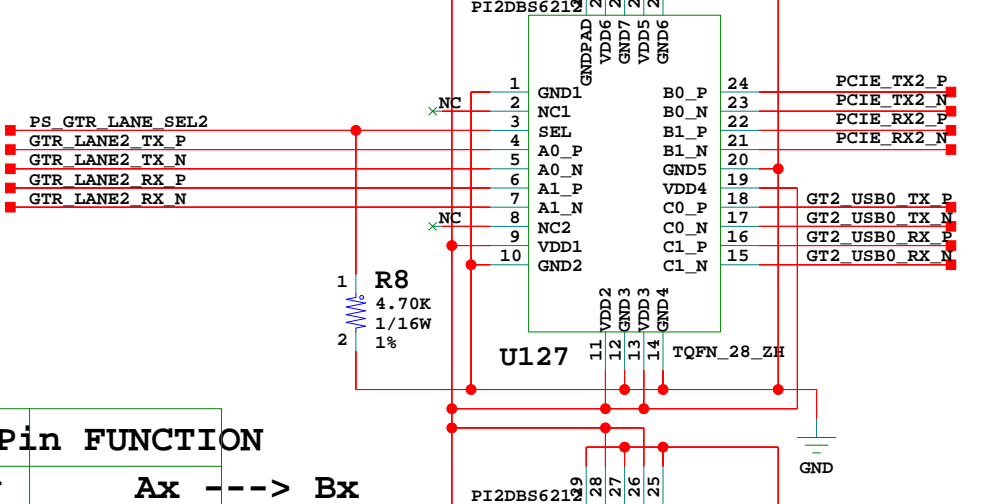
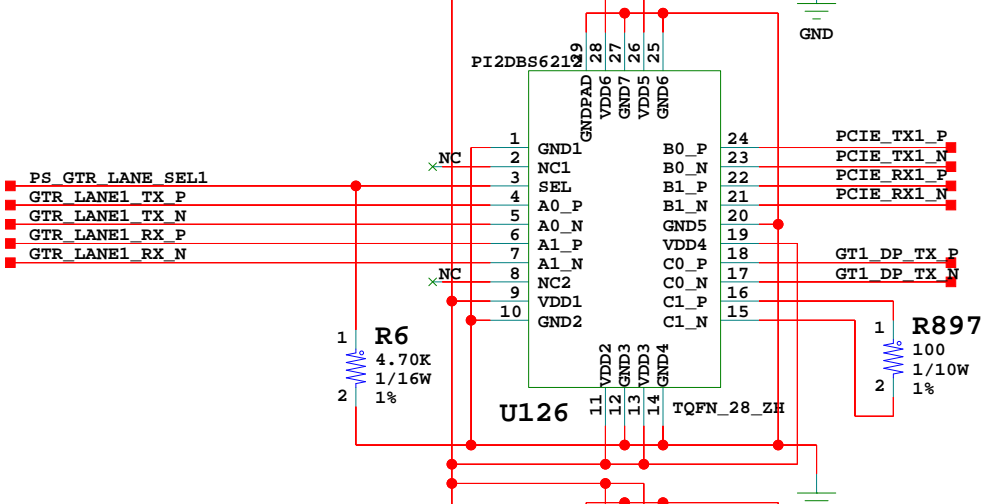
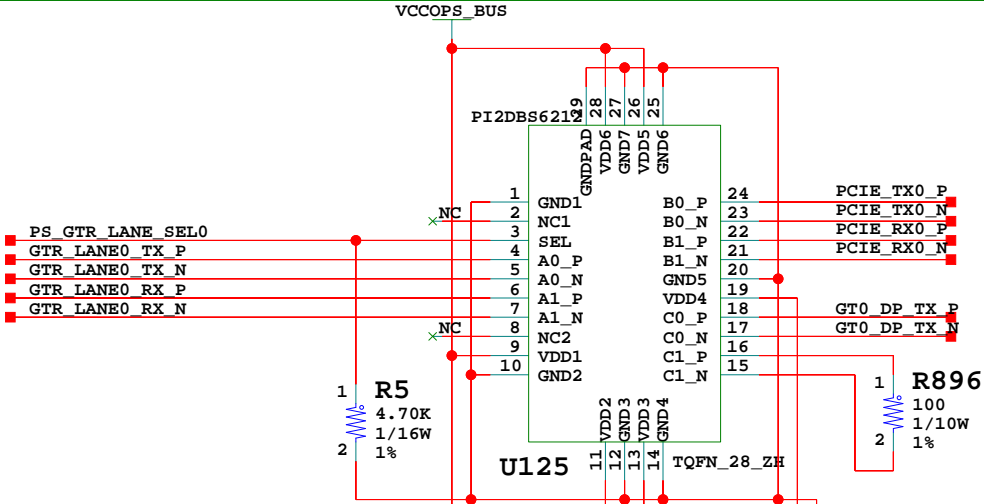
PS QSPI

			
TITLE: PS QSPI SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0		ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179	
DATE: 09/20/2016:10:27		VER:	1.0
SHEET SIZE: B		REV:	01
SHEET	46	OF	87
		DRAWN BY:	BF

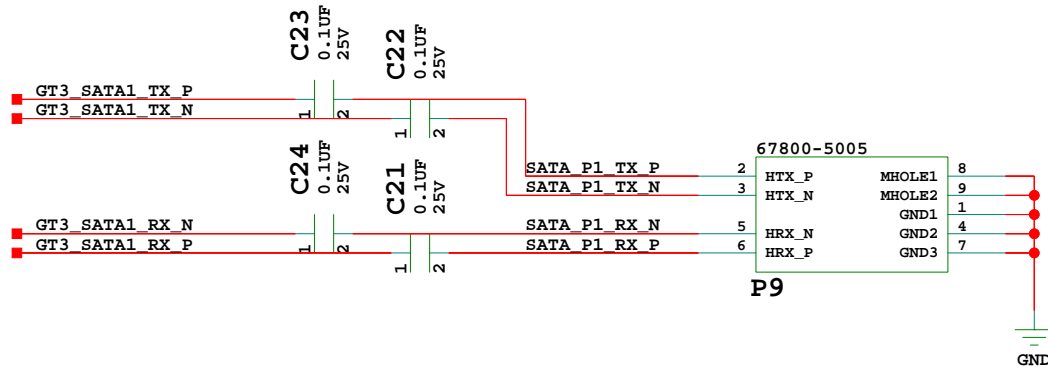
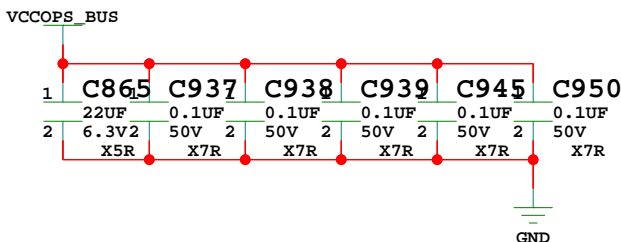
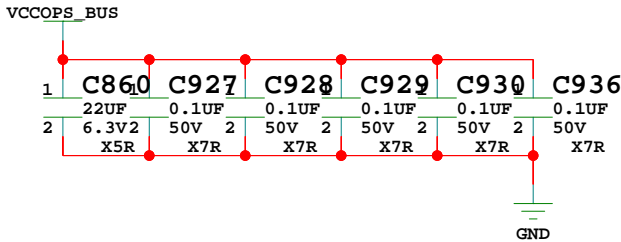
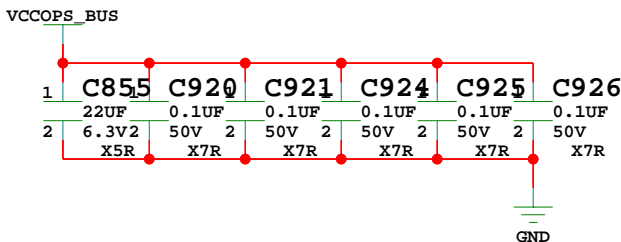
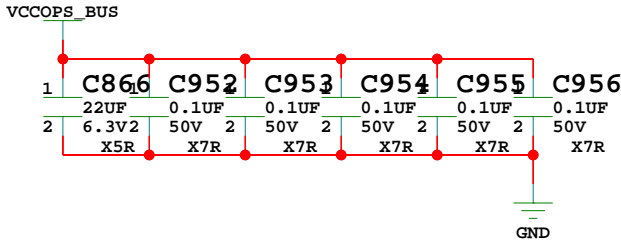


PS SD Card Connector

	
TITLE: PS SD Card Connector SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	
DATE: 09/20/2016:10:27	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 47 OF 87	DRAWN BY: BF



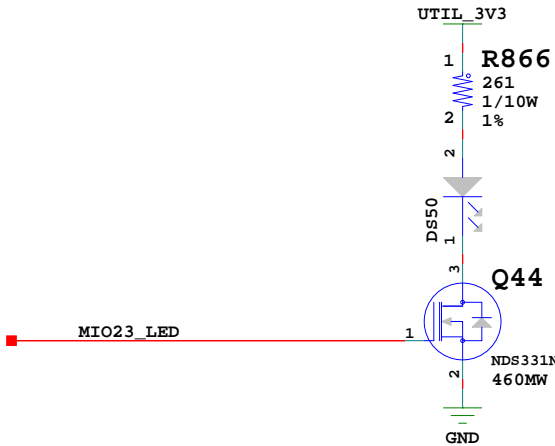
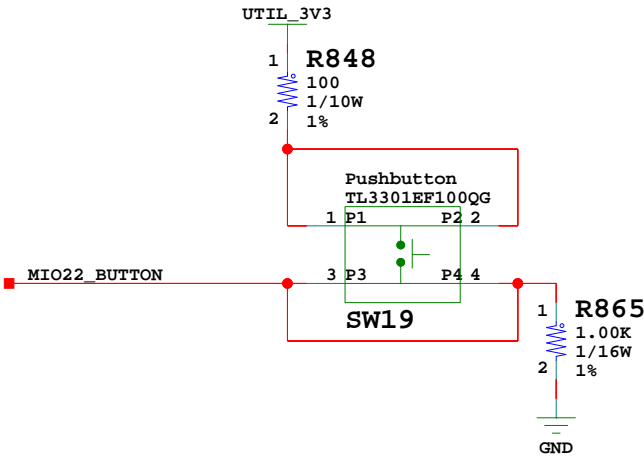
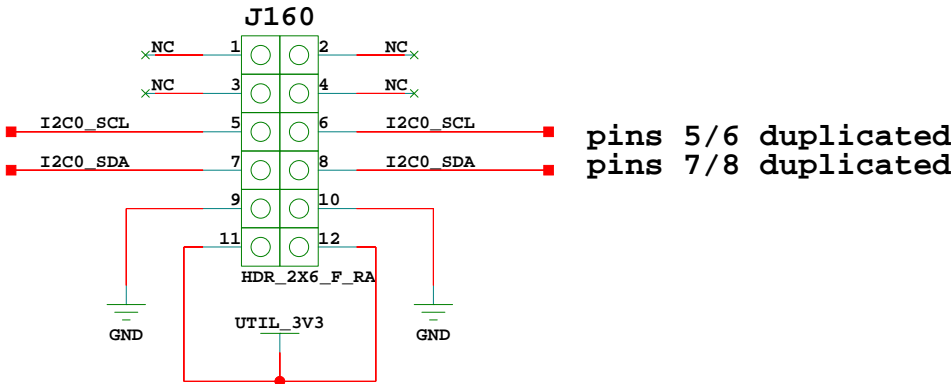
SEL Pin FUNCTION		
Low	Ax	---> Bx
High	Ax	---> Cx



PS GTR MUX - SATA

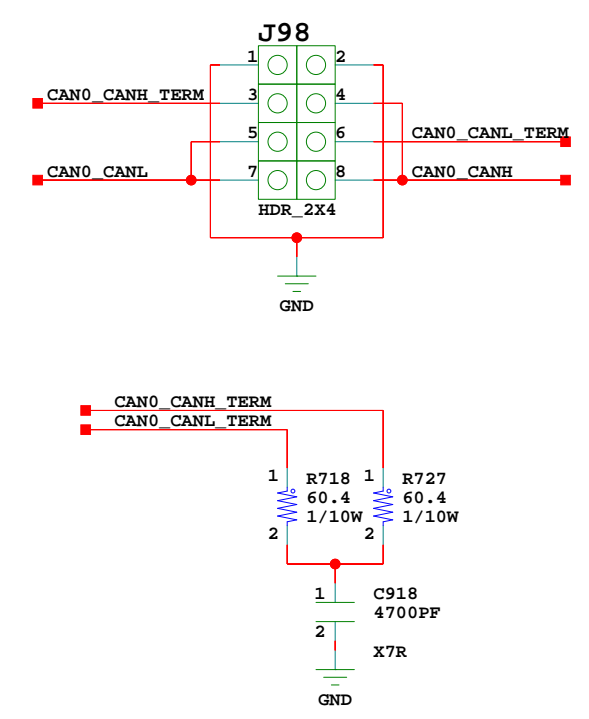
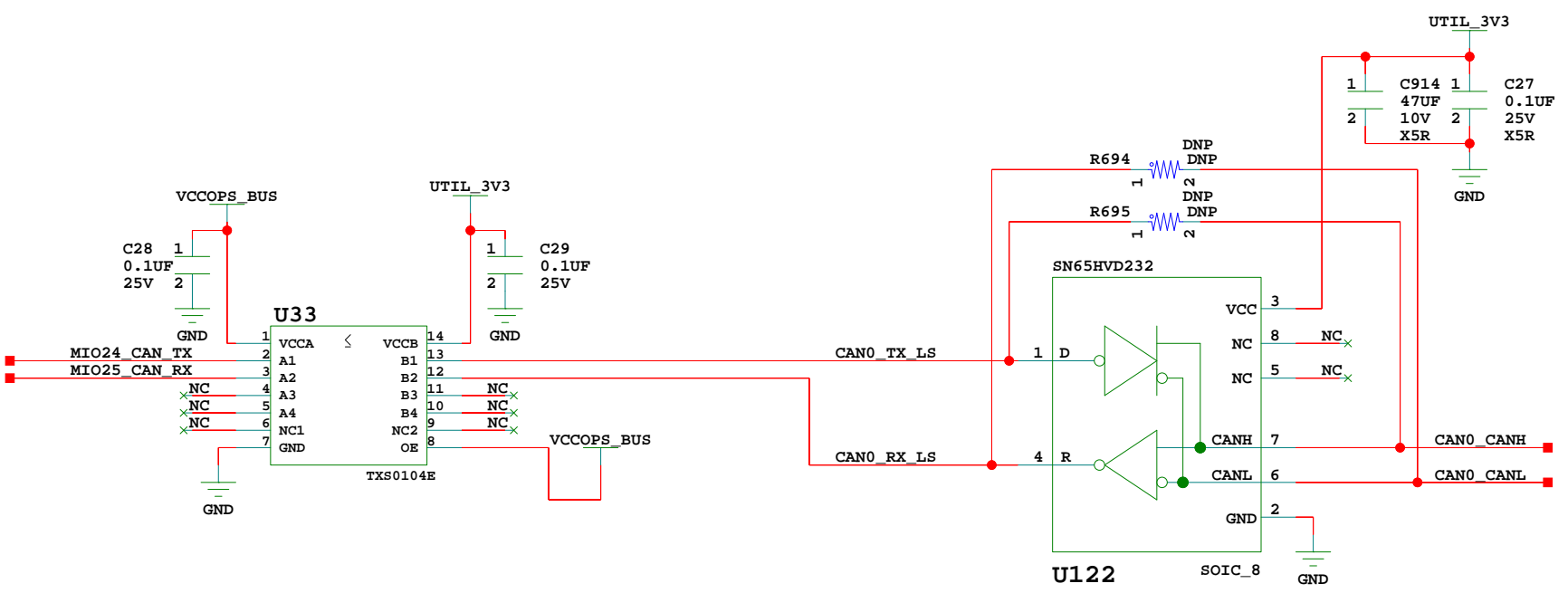
TITLE: PS GTR MUX - SATA SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	
ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179	
DATE: 09/20/2016:10:27	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 48 OF 87	DRAWN BY: BF

Connects to R.A. Female 2x6 PMOD receptacle



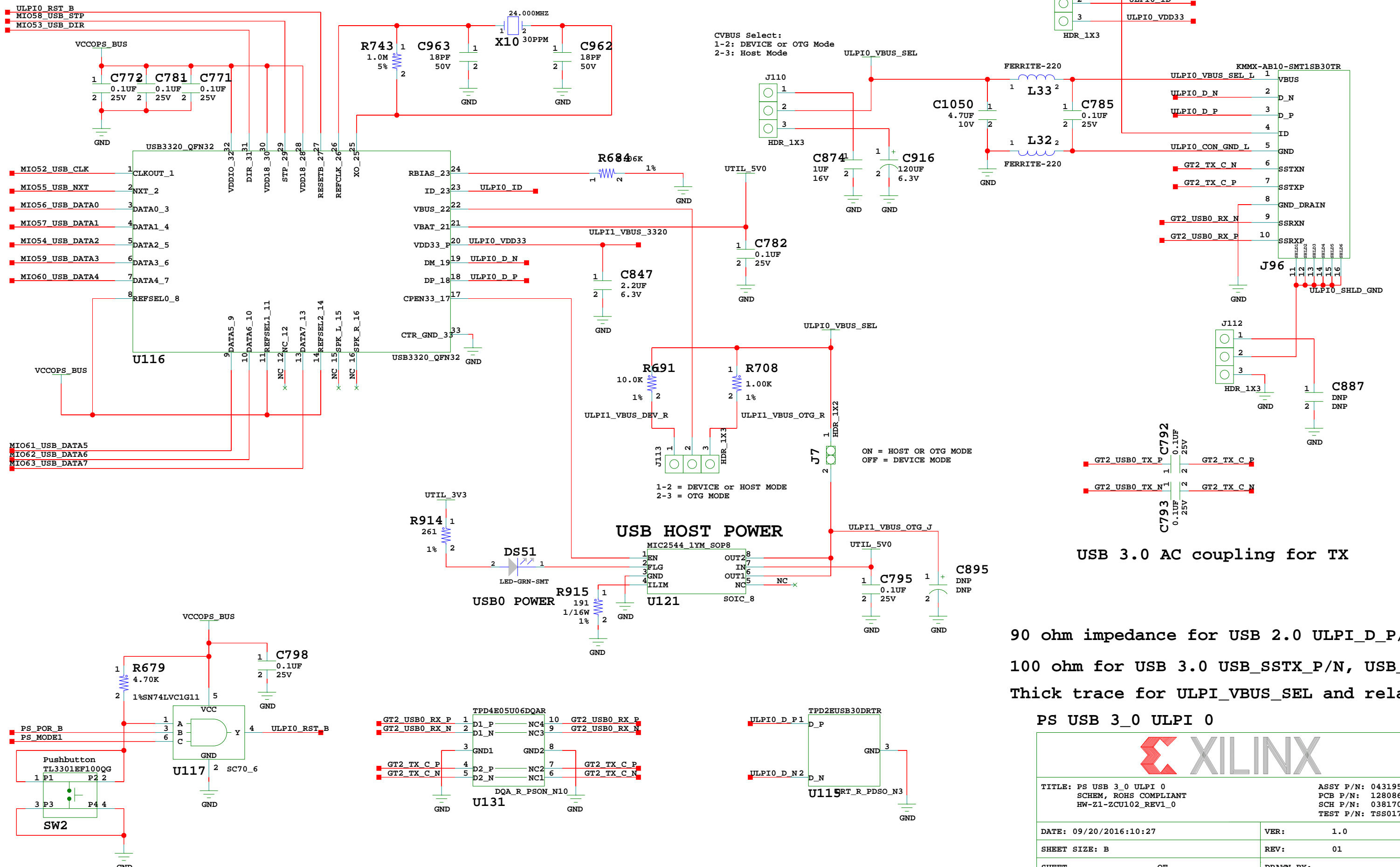
PS MIO PMOD - Button - LED

TITLE: PS MIO PMOD - Button - LED SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	
ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179	
DATE: 09/20/2016:10:27	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 49 OF 87	DRAWN BY: BF



PS CAN Bus

TITLE: PS CAN Bus SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0		ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179	
DATE: 09/20/2016:10:27	VER:	1.0	
SHEET SIZE: B	REV:	01	
SHEET 50 OF 87	DRAWN BY:	BF	

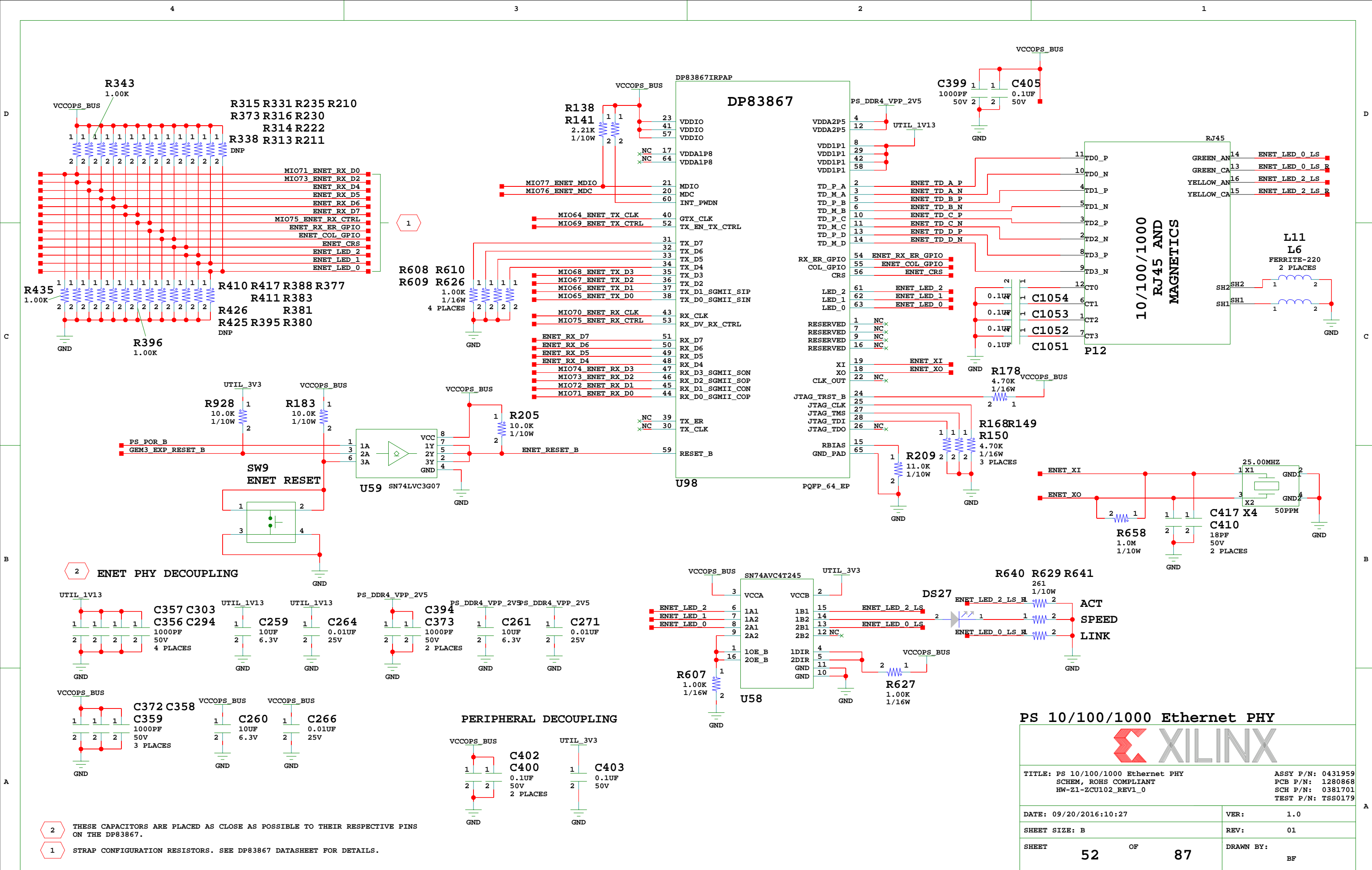


USB 3.0 AC coupling for TX

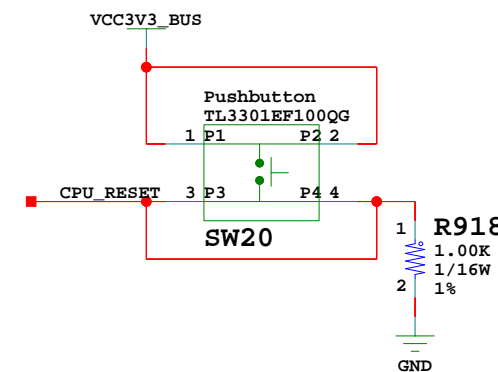
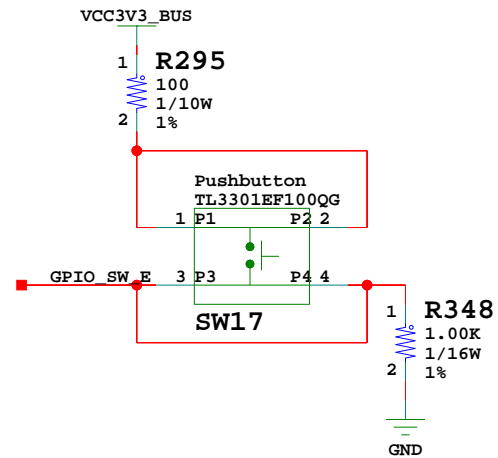
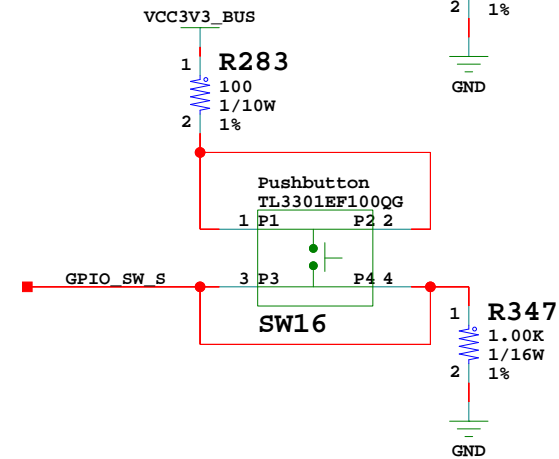
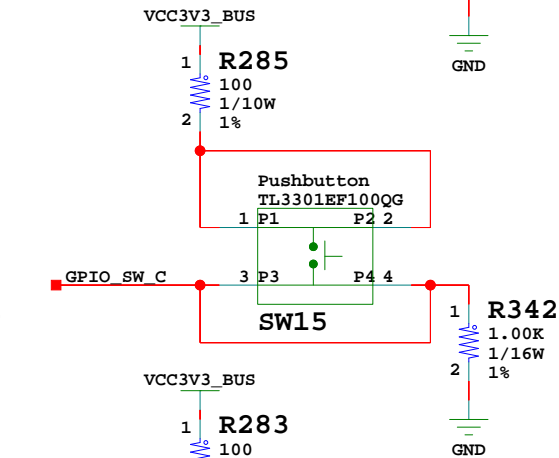
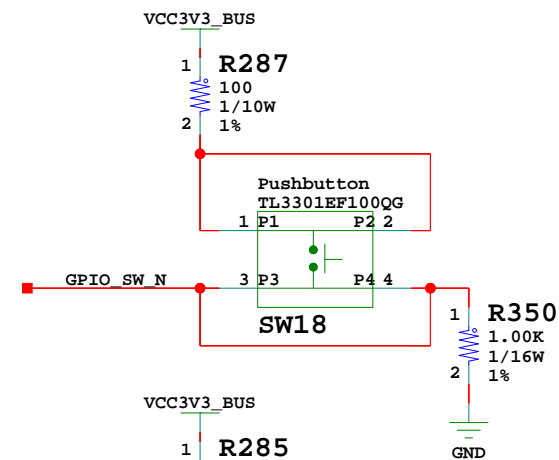
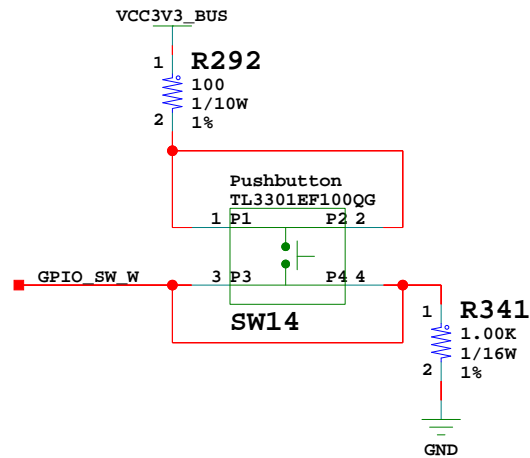
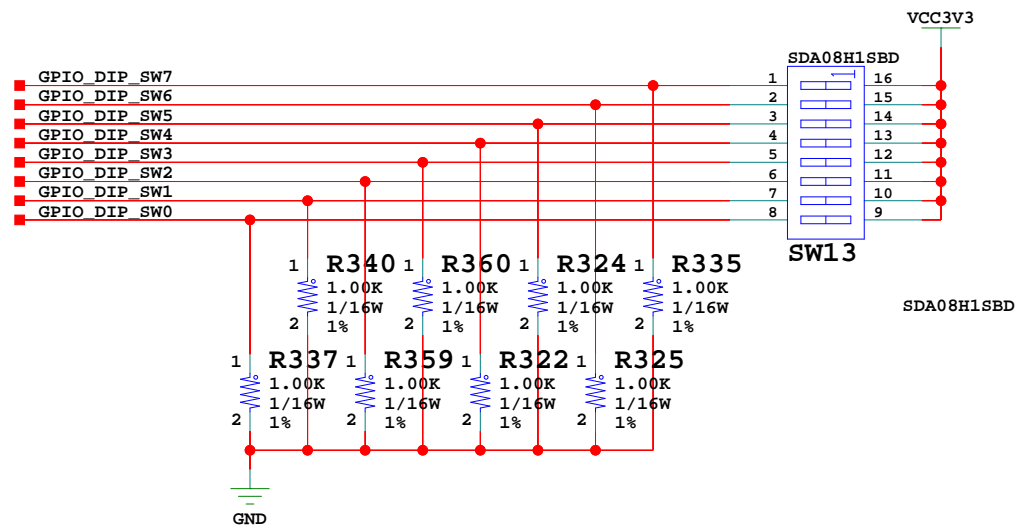
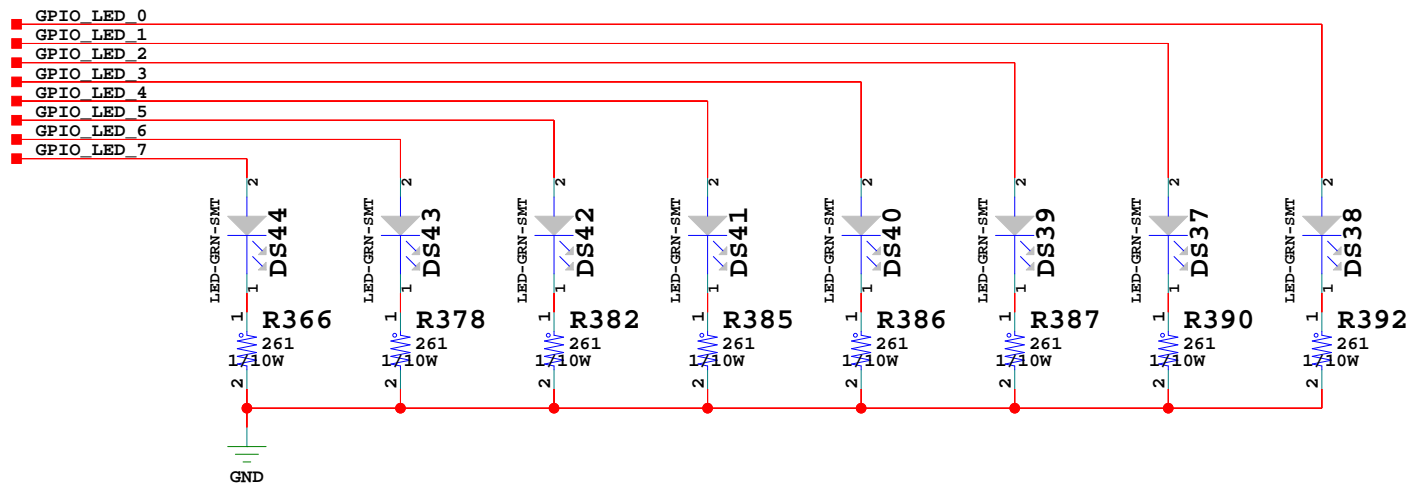
90 ohm impedance for USB 2.0 ULPI_D_P/N,
100 ohm for USB 3.0 USB_SSTX_P/N, USB_SSRX_P/N
Thick trace for ULPI_VBUS_SEL and related

PS USB 3_0 ULPI 0

TITLE: PS USB 3_0 ULPI 0 SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	
ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179	
DATE: 09/20/2016:10:27	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 51 OF 87	DRAWN BY: BF



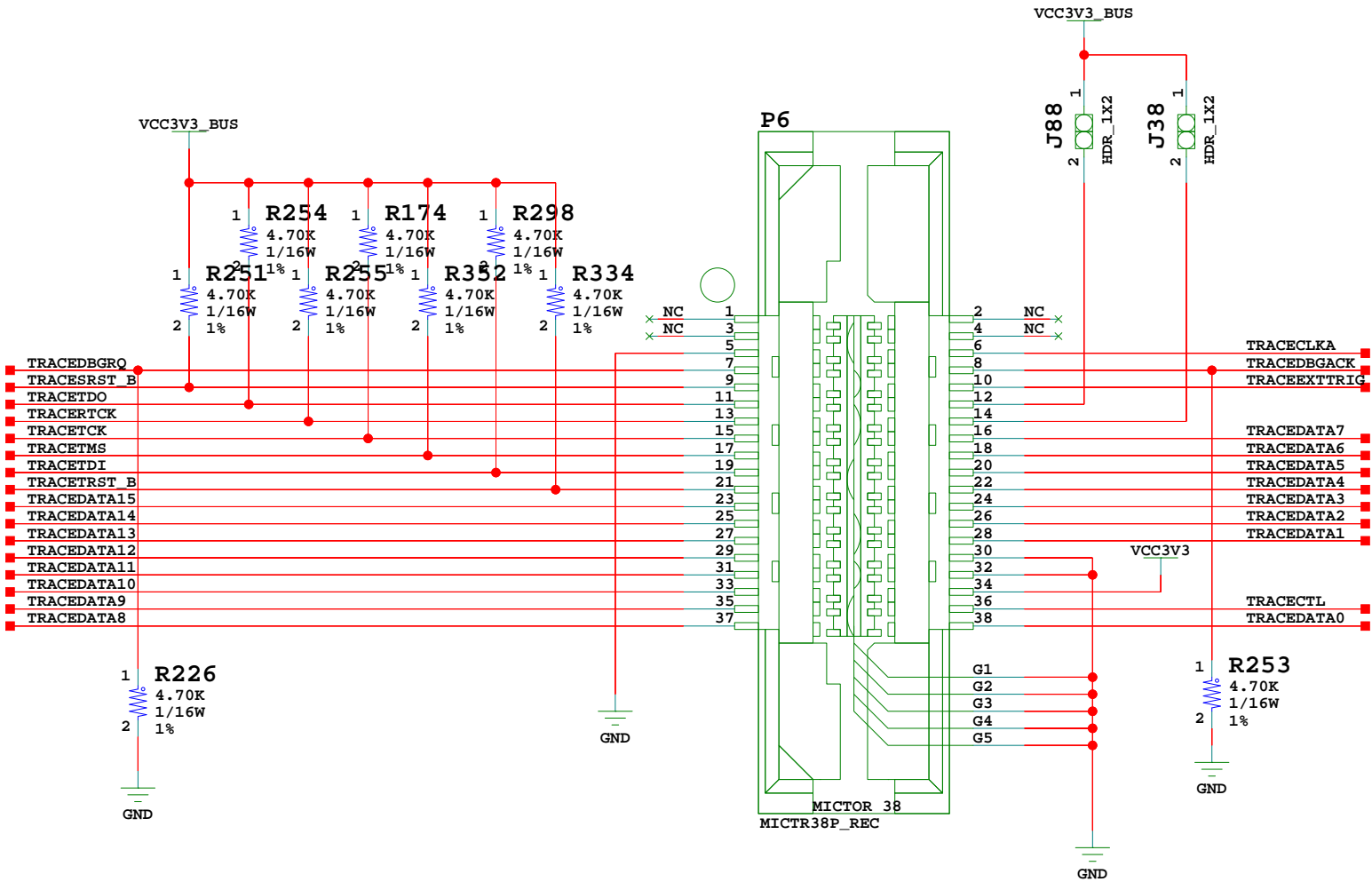
LEDs near top right edge



PL Buttons - Switches - LEDs

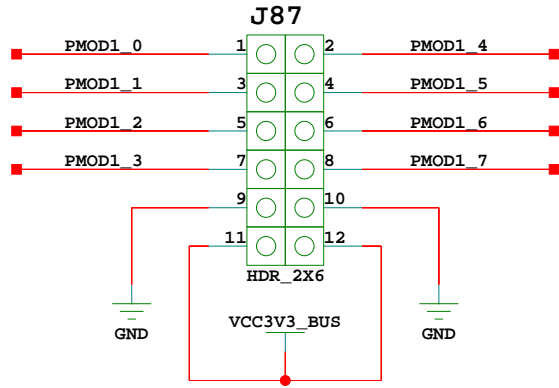
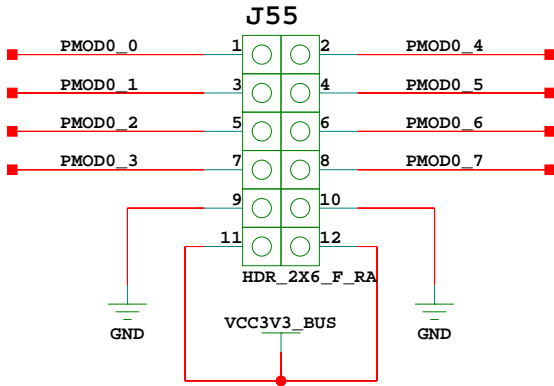
TITLE: PL Buttons - Switches - LEDs SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	
ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179	
DATE: 09/20/2016:10:27	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 53 OF 87	DRAWN BY: BF

EMIO ARM Trace/Debug



PL EMIO ARM Trace Debug

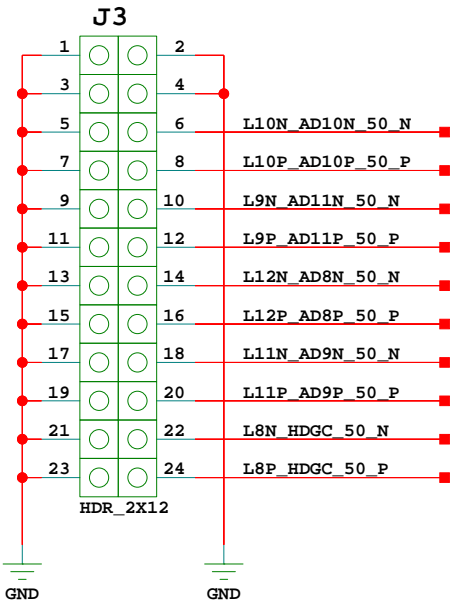
TITLE: PL EMIO ARM Trace Debug SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0		ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179	
DATE: 09/20/2016:10:27		VER:	1.0
SHEET SIZE: B		REV:	01
SHEET	54	OF	87
		DRAWN BY:	BF



PL PMODs

TITLE: PL PMODs SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0		ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179	
DATE: 09/20/2016:10:27		VER:	1.0
SHEET SIZE: B		REV:	01
SHEET	55	OF	87
		DRAWN BY:	BF

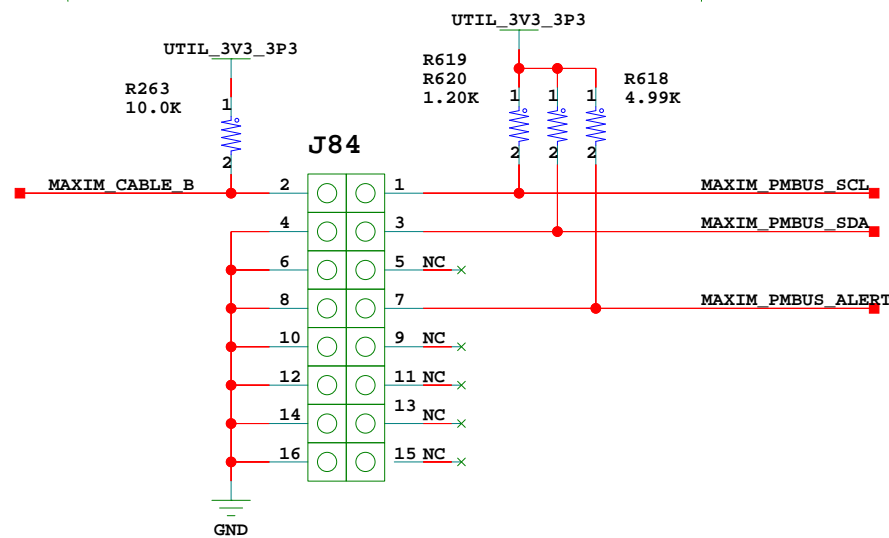
Prototype Header



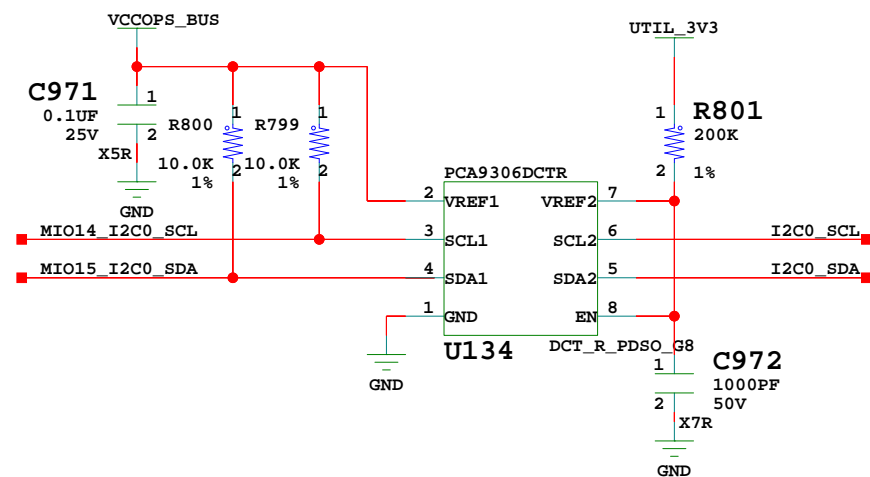
PL SYSMON Prototype Header

TITLE: PL SYSMON Prototype Header SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0		ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179	
DATE: 09/20/2016:10:27		VER:	1.0
SHEET SIZE: B		REV:	02
SHEET	56	OF	87
		DRAWN BY:	BF

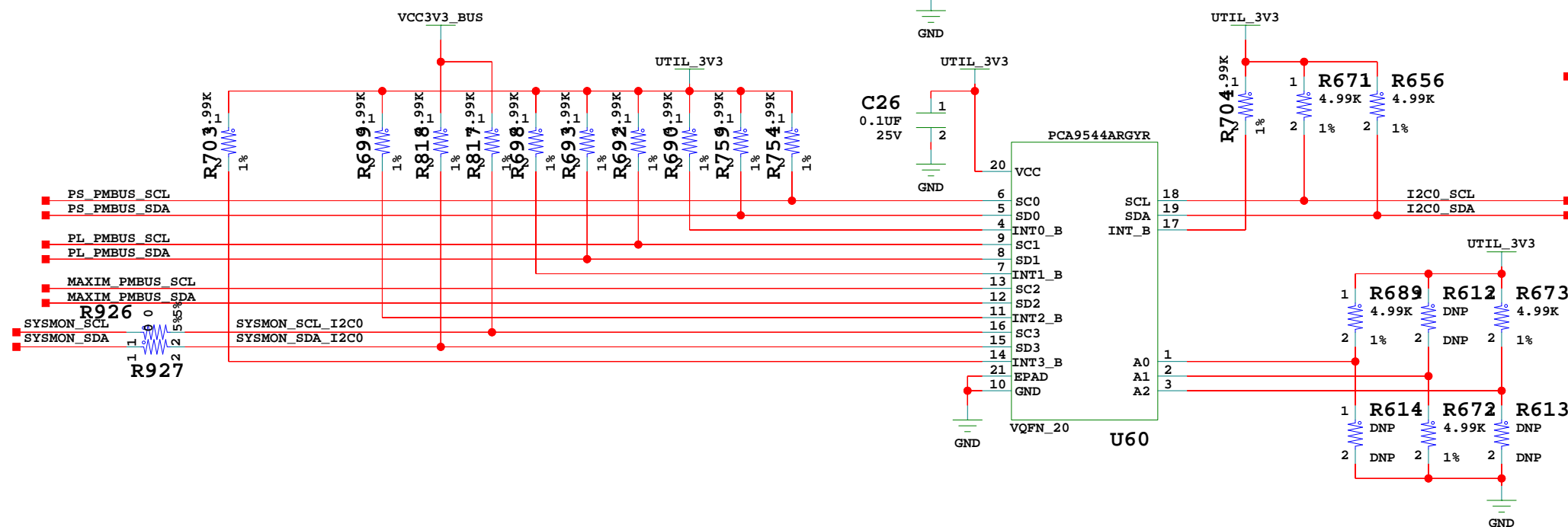
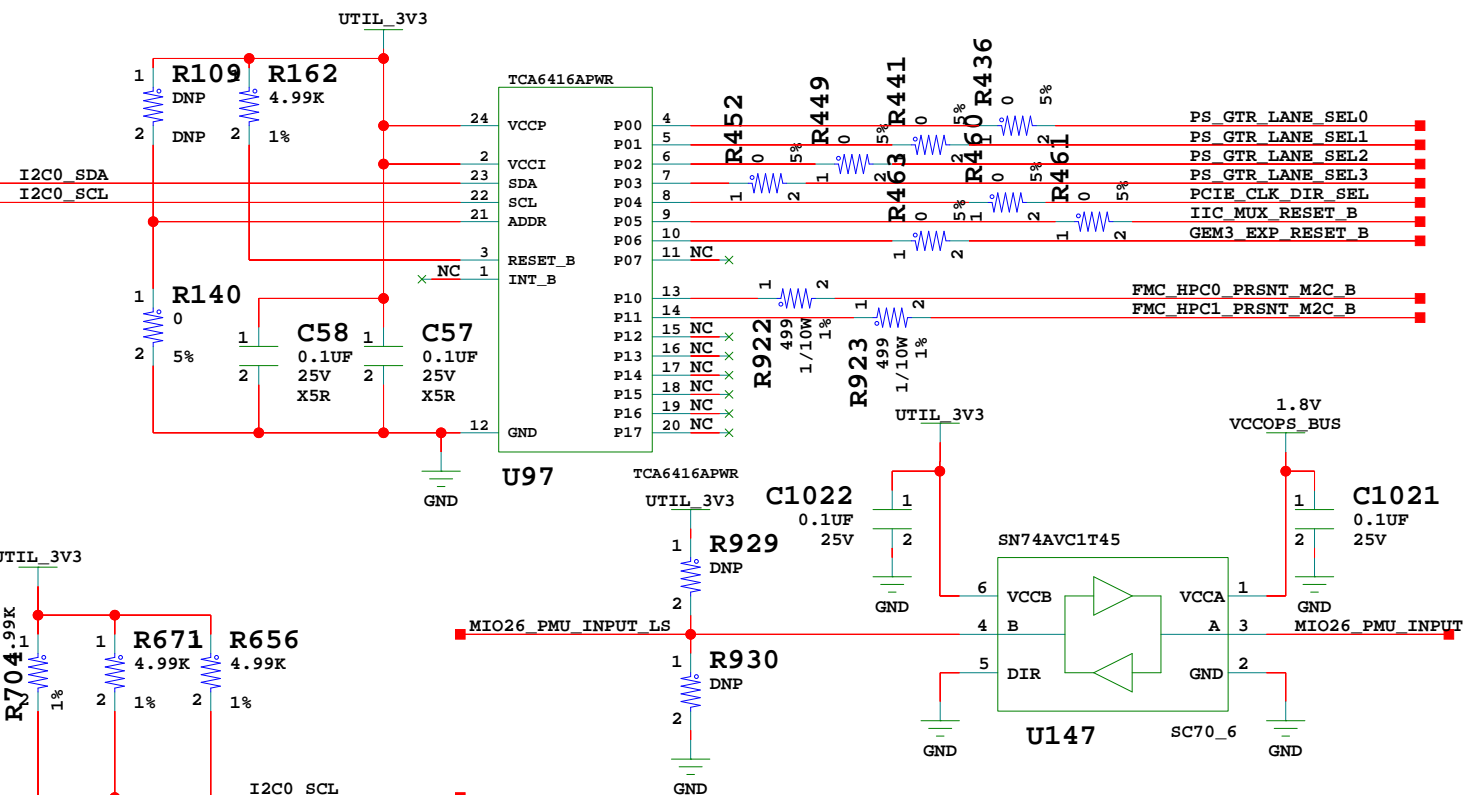
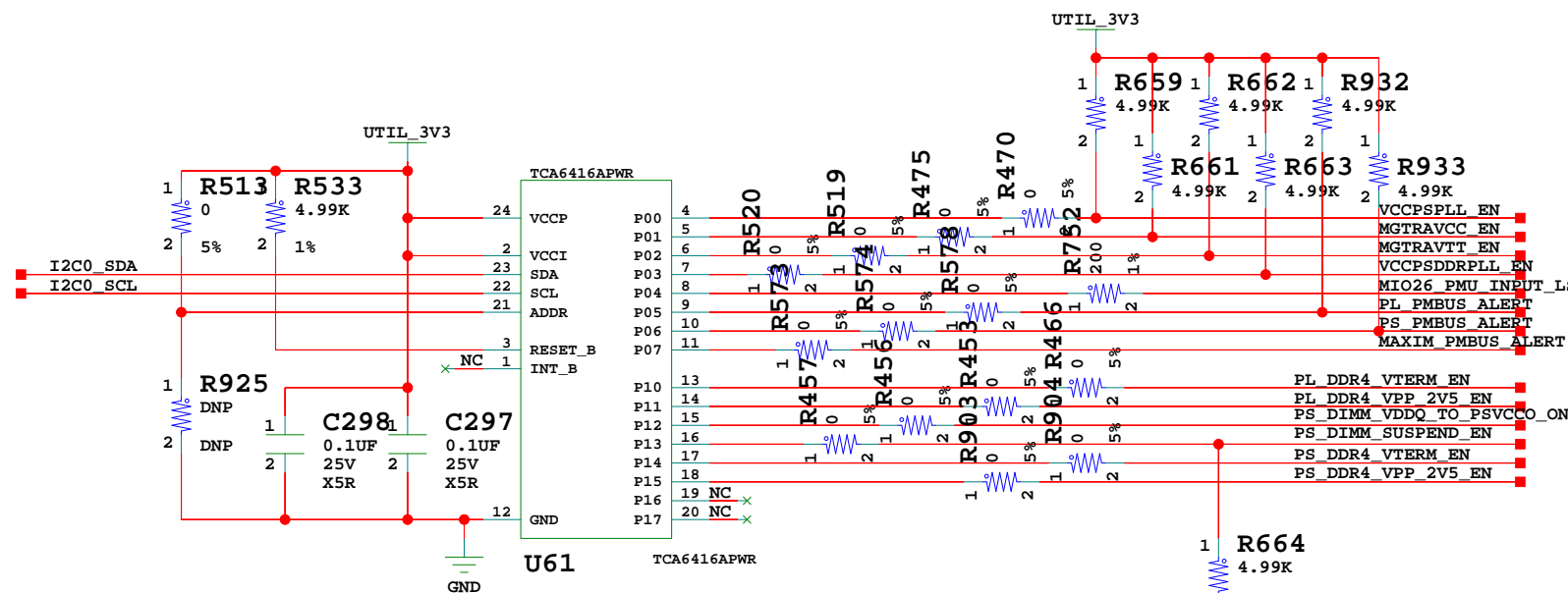
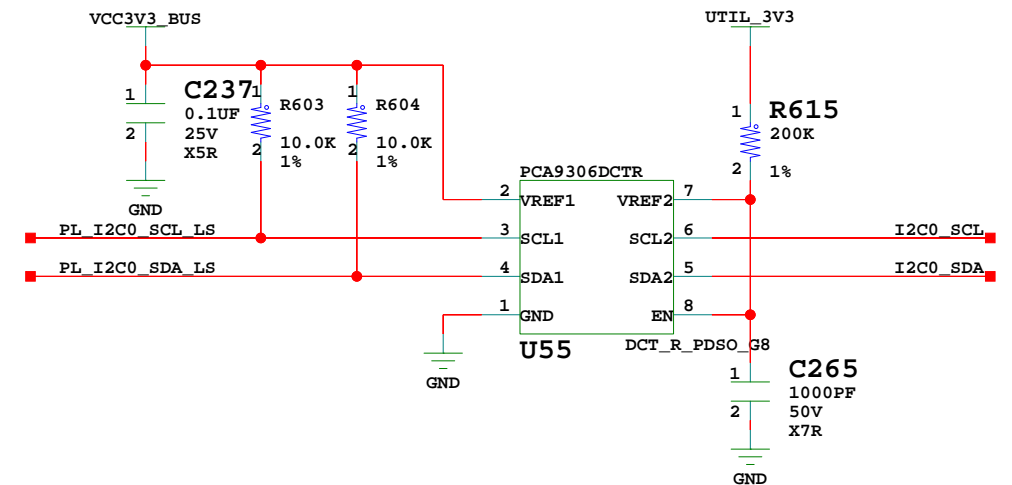
MAXIM PMBUS PROGRAMMING CABLE



PS I2C Level Shifter (I2C0)



PL I2C Level Shifter (disabled if VCC3V3 is off)

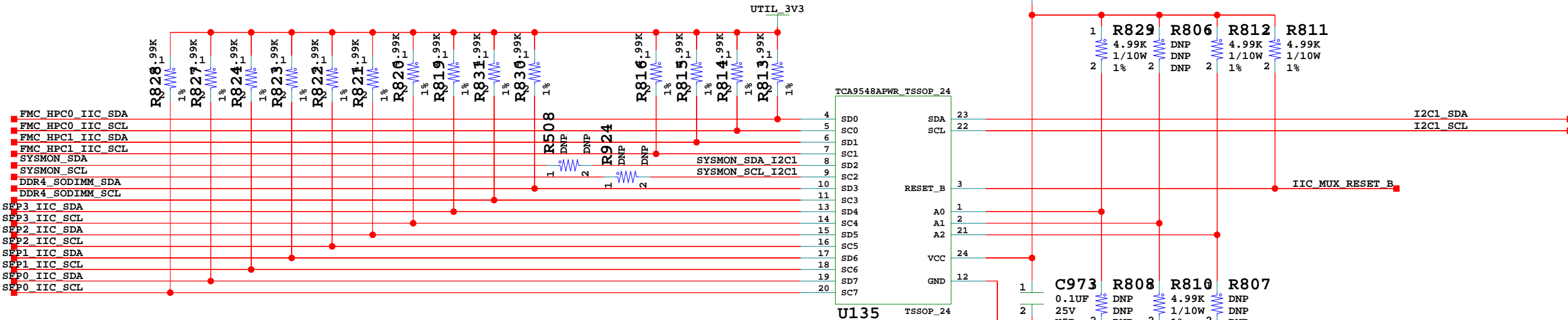
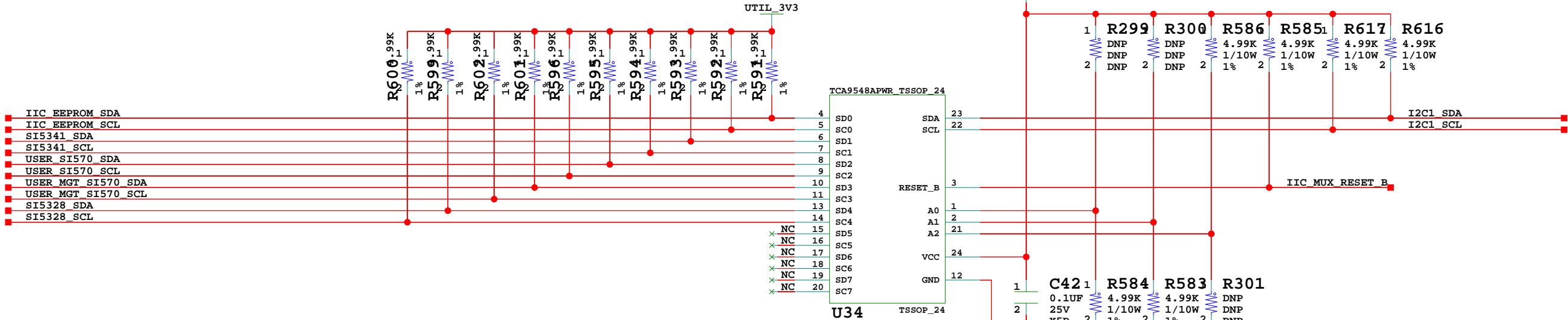


I2C0 MUXes Expanders Level Shifters PMBUS H

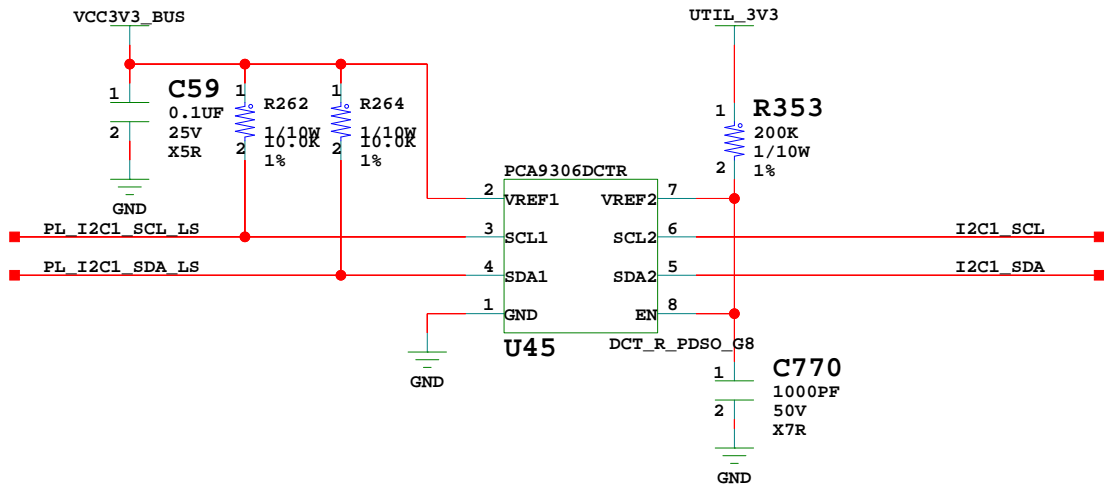


TITLE: I2C0 MUXES Expanders Level Shifters PMBUS Headers	ASSY P/N: 0431959
SCHEM, ROHS COMPLIANT	PCB P/N: 1280868
HW-Z1-ZCU102_REV1_0	SCH P/N: 0381701
	TEST P/N: TSS0179

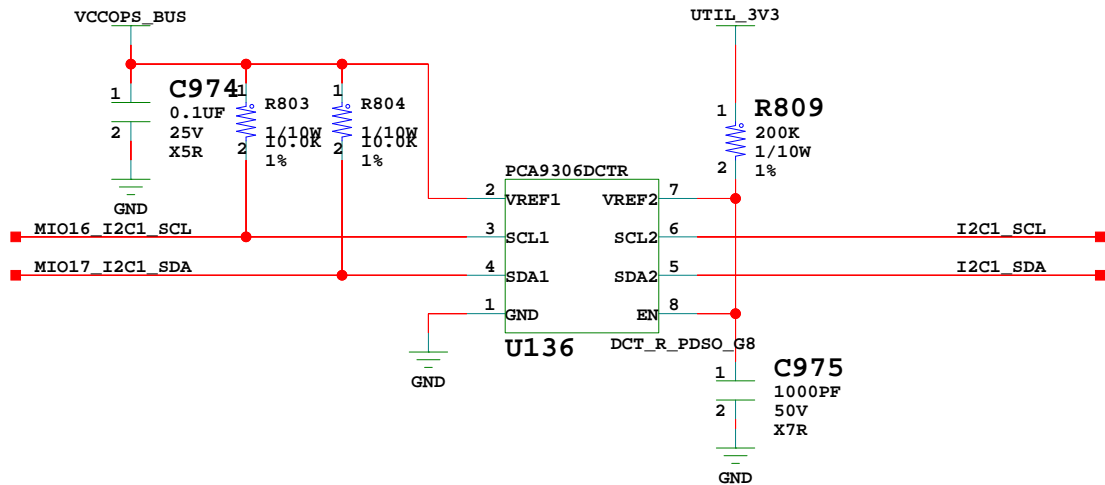
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 57 OF 87	DRAWN BY: BF



PL I2C Level Shifter (disabled if VCC3V3 is off)



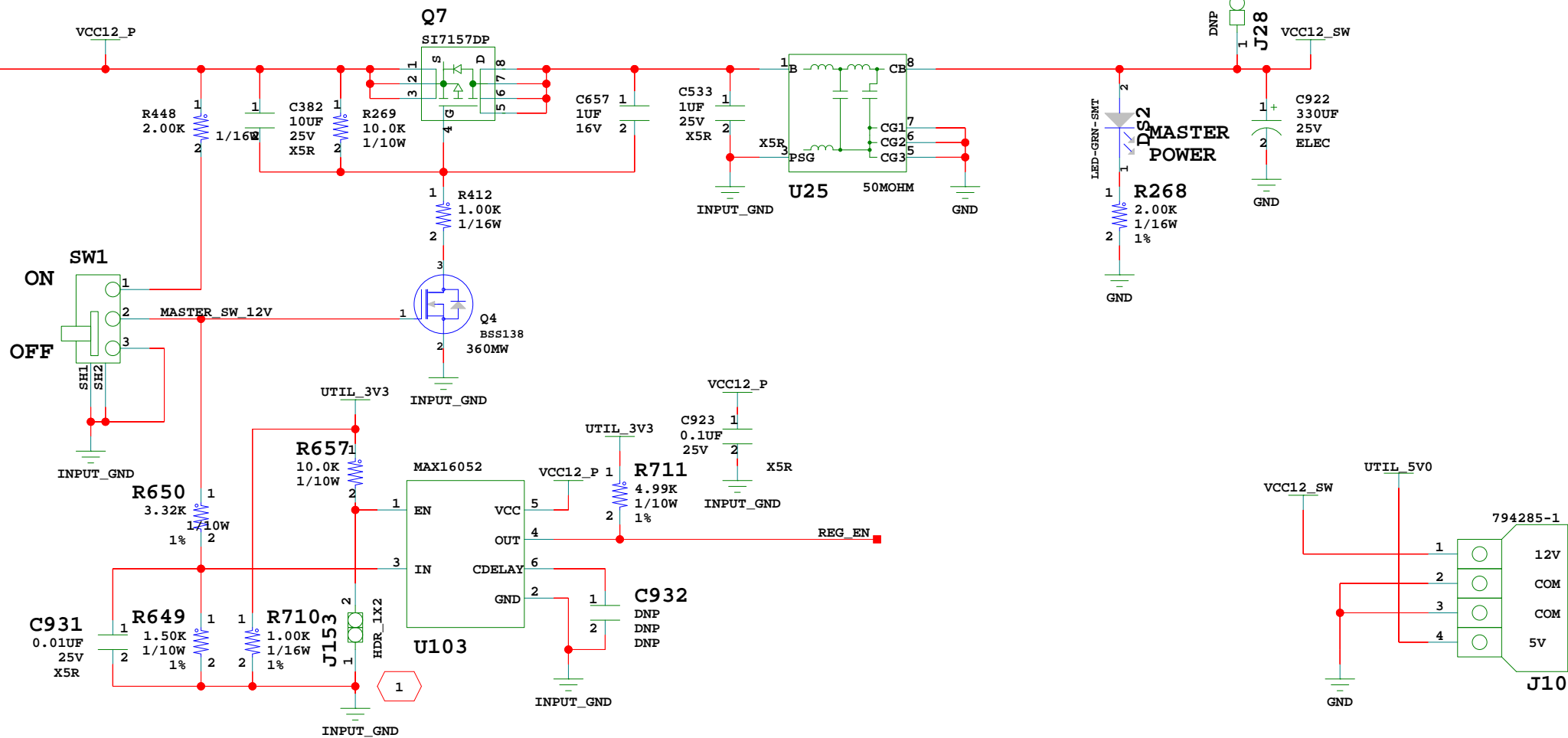
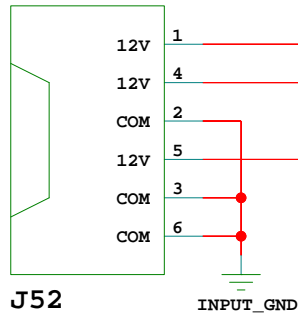
PS I2C Level Shifter (I2C1)



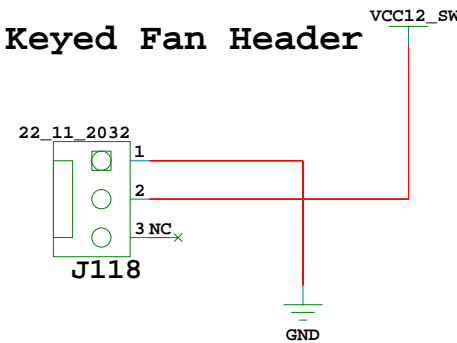
I2C1 MUXes and Level Shifters

TITLE: I2C1 MUXes and Level Shifters SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 58 OF 87	DRAWN BY: BF

6-PIN MINI-FIT
AC ADAPTER (BRICK)



Keyed Fan Header



12V Power Connectors Switch



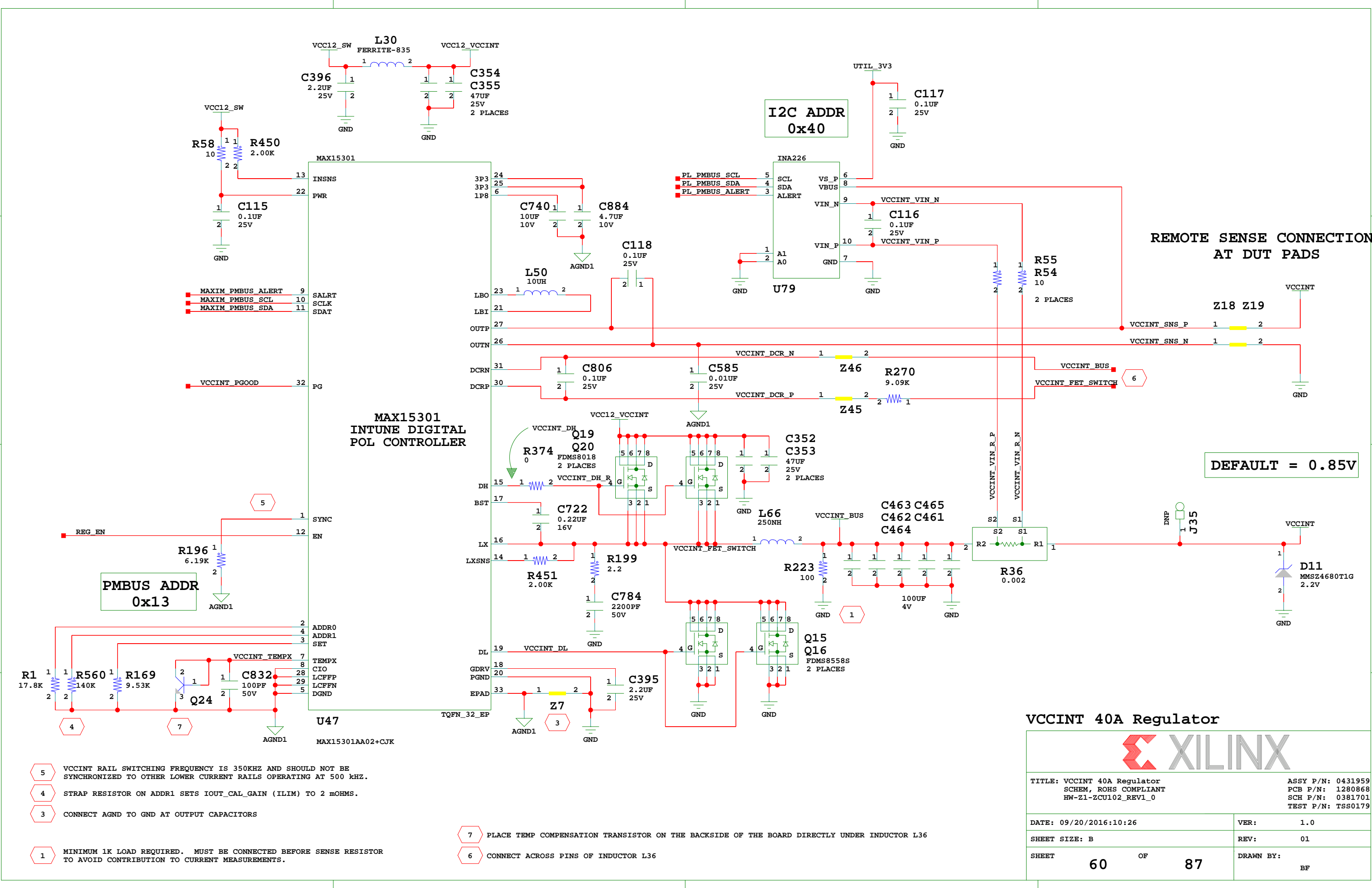
TITLE: 12V Power Connectors Switch
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU102_REV1_0

ASSY P/N: 0431959
PCB P/N: 1280868
SCH P/N: 0381701
TEST P/N: TSS0179

DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 59 OF 87	DRAWN BY: BF

GND Test points

1 Maxim Regulator Inhibit Jumper



REMOTE SENSE CONNECTIONS
AT DUT PADS

DEFAULT = 0.85V

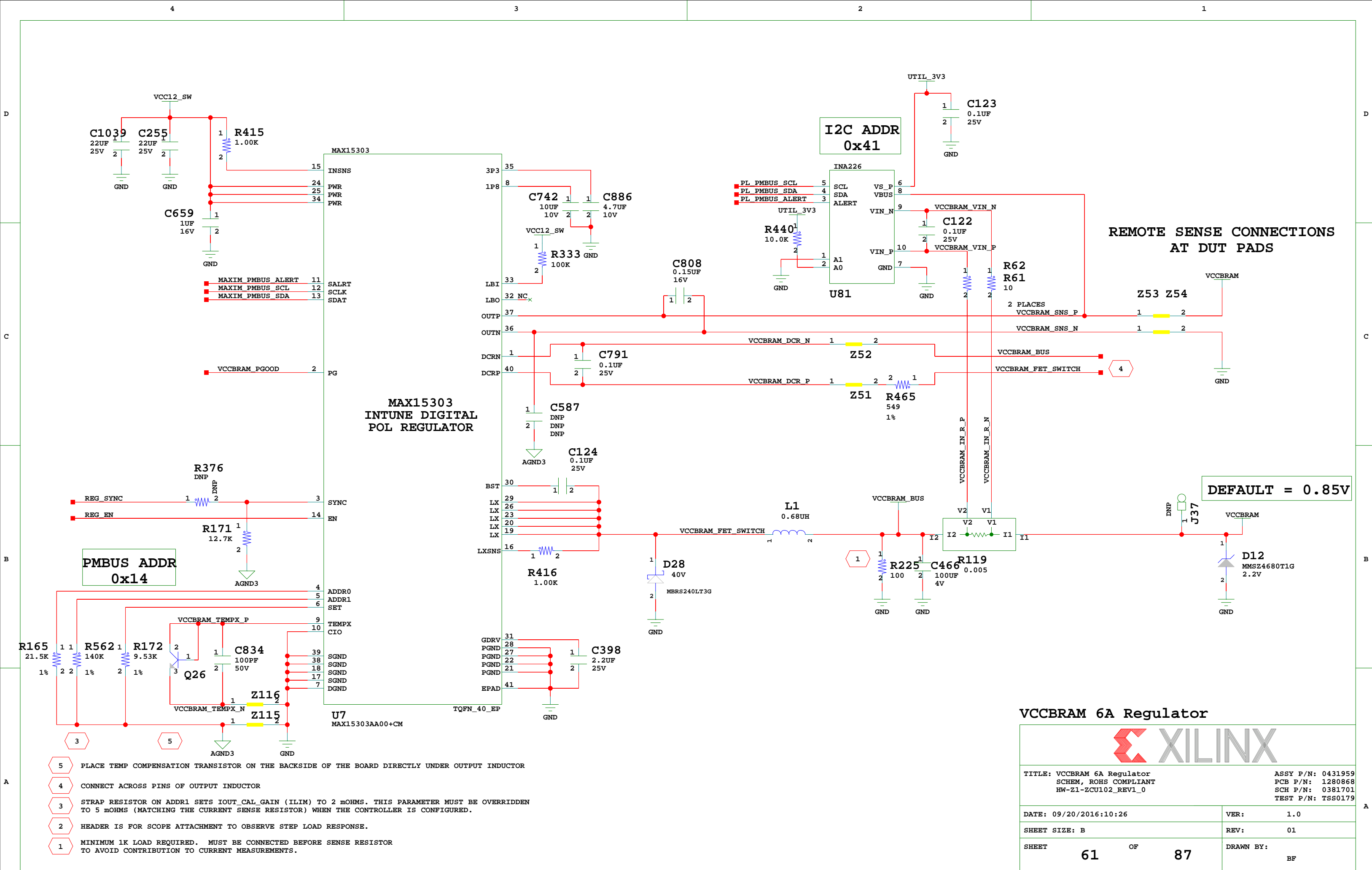
VCCINT 40A Regulator

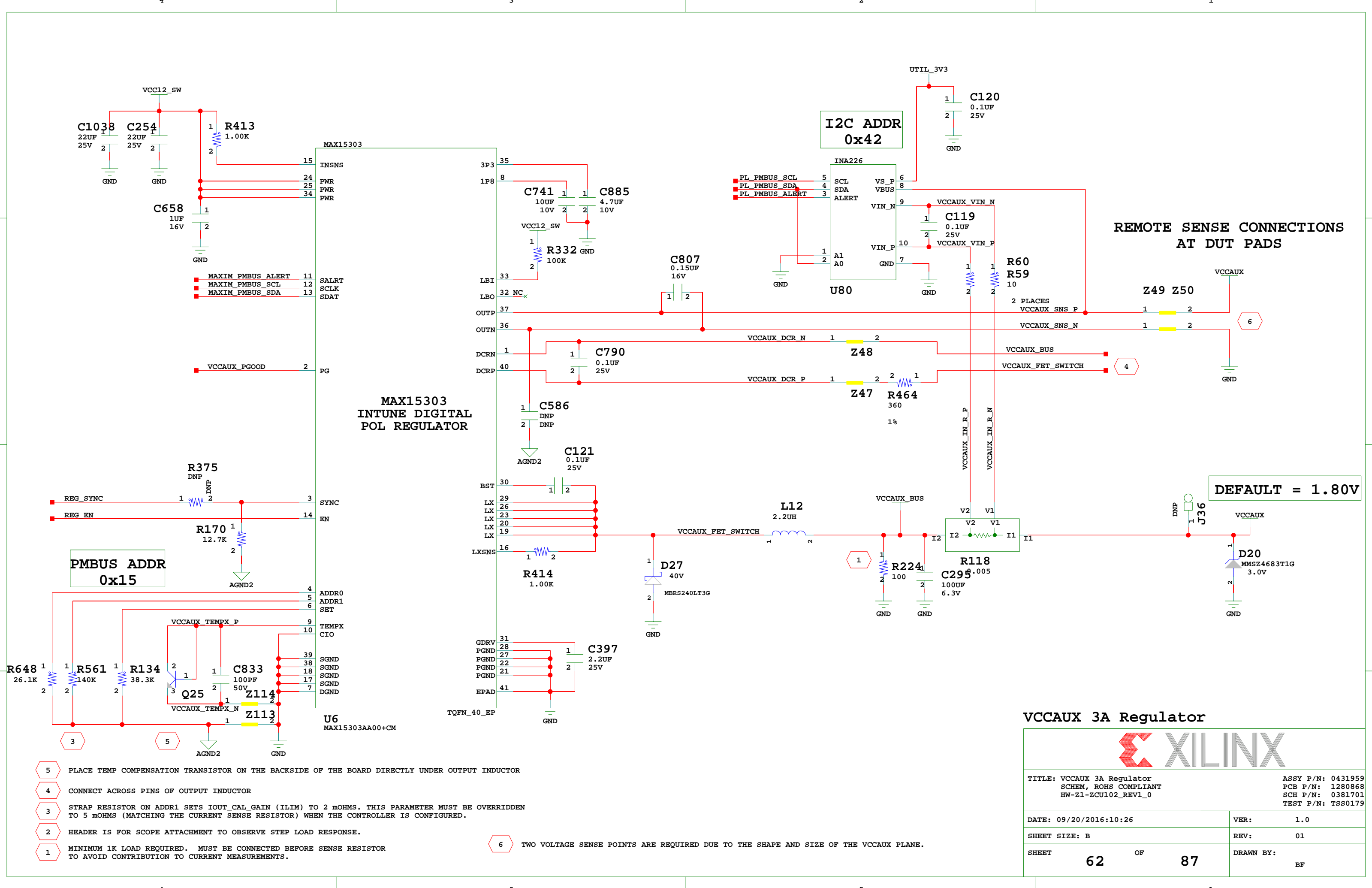


TITLE: VCCINT 40A Regulator SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
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DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 60 OF 87	DRAWN BY: BF

- 5 VCCINT RAIL SWITCHING FREQUENCY IS 350KHZ AND SHOULD NOT BE SYNCHRONIZED TO OTHER LOWER CURRENT RAILS OPERATING AT 500 KHZ.
- 4 STRAP RESISTOR ON ADDR1 SETS IOUT_CAL_GAIN (ILIM) TO 2 MOHMS.
- 3 CONNECT AGND TO GND AT OUTPUT CAPACITORS
- 7 PLACE TEMP COMPENSATION TRANSISTOR ON THE BACKSIDE OF THE BOARD DIRECTLY UNDER INDUCTOR L36
- 6 CONNECT ACROSS PINS OF INDUCTOR L36
- 1 MINIMUM 1K LOAD REQUIRED. MUST BE CONNECTED BEFORE SENSE RESISTOR TO AVOID CONTRIBUTION TO CURRENT MEASUREMENTS.





MAX15303
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POL REGULATOR

I2C ADDR
0x42

REMOTE SENSE CONNECTIONS
AT DUT PADS

DEFAULT = 1.80V

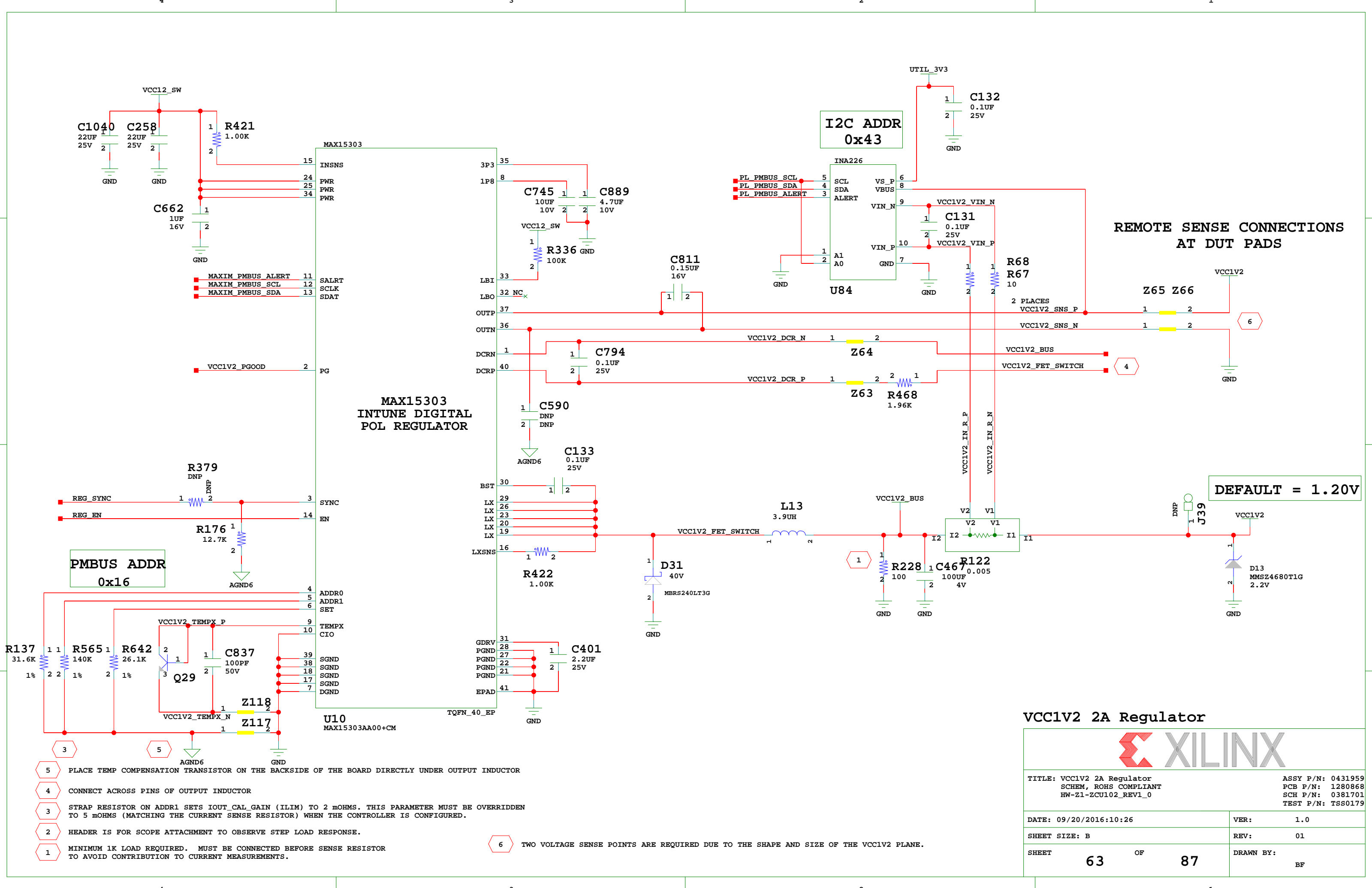
VCCAUX 3A Regulator



TITLE: VCCAUX 3A Regulator SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
--	--

DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 62 OF 87	DRAWN BY: BF

- 5 PLACE TEMP COMPENSATION TRANSISTOR ON THE BACKSIDE OF THE BOARD DIRECTLY UNDER OUTPUT INDUCTOR
- 4 CONNECT ACROSS PINS OF OUTPUT INDUCTOR
- 3 STRAP RESISTOR ON ADDR1 SETS IOUT_CAL_GAIN (ILIM) TO 2 mOHMS. THIS PARAMETER MUST BE OVERRIDDEN TO 5 mOHMS (MATCHING THE CURRENT SENSE RESISTOR) WHEN THE CONTROLLER IS CONFIGURED.
- 2 HEADER IS FOR SCOPE ATTACHMENT TO OBSERVE STEP LOAD RESPONSE.
- 1 MINIMUM 1K LOAD REQUIRED. MUST BE CONNECTED BEFORE SENSE RESISTOR TO AVOID CONTRIBUTION TO CURRENT MEASUREMENTS.
- 6 TWO VOLTAGE SENSE POINTS ARE REQUIRED DUE TO THE SHAPE AND SIZE OF THE VCCAUX PLANE.



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REMOTE SENSE CONNECTIONS
AT DUT PADS

DEFAULT = 1.20V

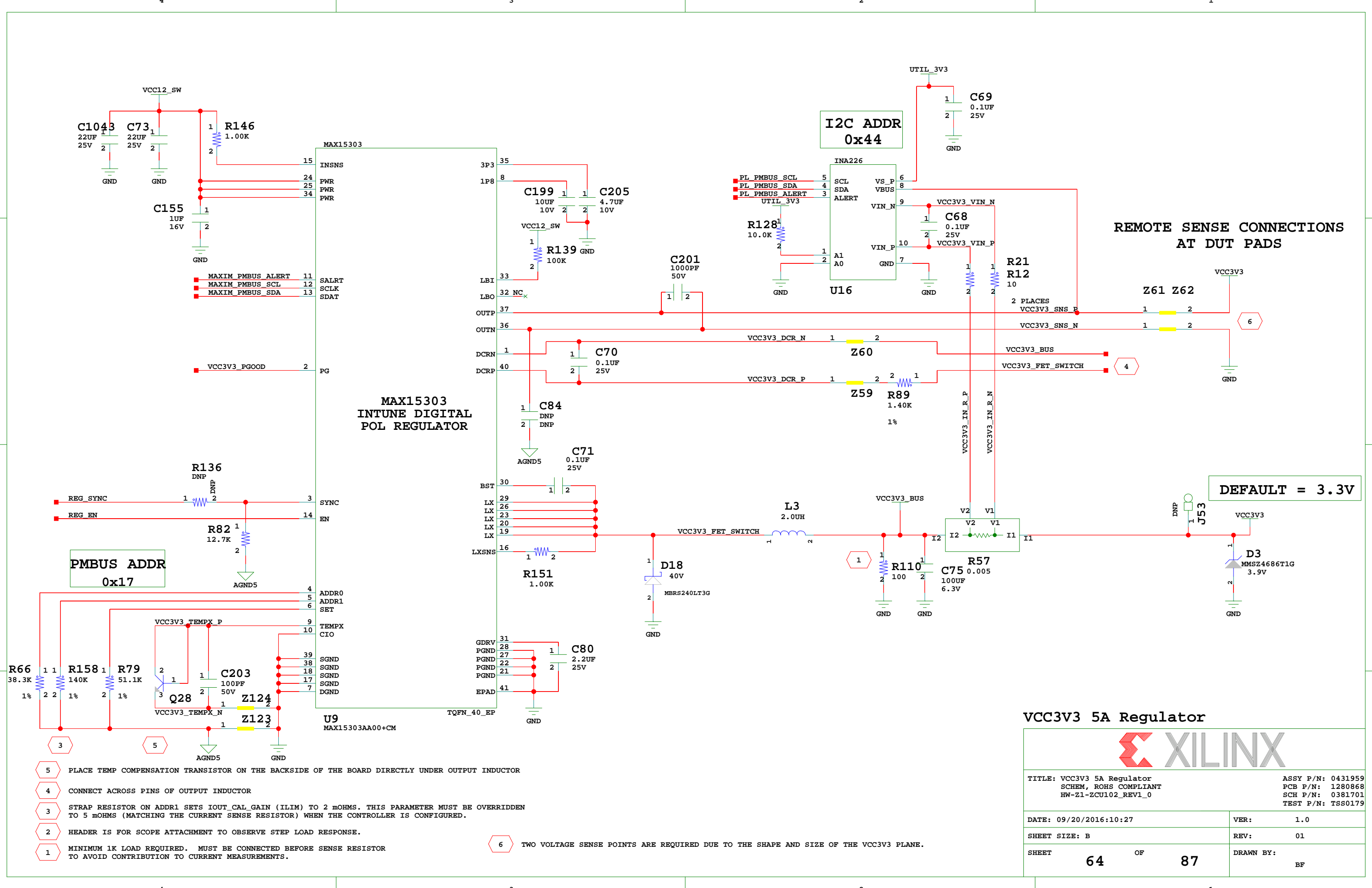
VCC1V2 2A Regulator



TITLE: VCC1V2 2A Regulator SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
--	--

DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 63 OF 87	DRAWN BY: BF

- 5 PLACE TEMP COMPENSATION TRANSISTOR ON THE BACKSIDE OF THE BOARD DIRECTLY UNDER OUTPUT INDUCTOR
- 4 CONNECT ACROSS PINS OF OUTPUT INDUCTOR
- 3 STRAP RESISTOR ON ADDR1 SETS IOUT_CAL_GAIN (ILIM) TO 2 mOHMS. THIS PARAMETER MUST BE OVERRIDDEN TO 5 mOHMS (MATCHING THE CURRENT SENSE RESISTOR) WHEN THE CONTROLLER IS CONFIGURED.
- 2 HEADER IS FOR SCOPE ATTACHMENT TO OBSERVE STEP LOAD RESPONSE.
- 1 MINIMUM 1K LOAD REQUIRED. MUST BE CONNECTED BEFORE SENSE RESISTOR TO AVOID CONTRIBUTION TO CURRENT MEASUREMENTS.
- 6 TWO VOLTAGE SENSE POINTS ARE REQUIRED DUE TO THE SHAPE AND SIZE OF THE VCC1V2 PLANE.



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INTUNE DIGITAL
POL REGULATOR

REMOTE SENSE CONNECTIONS
AT DUT PADS

DEFAULT = 3.3V

VCC3V3 5A Regulator

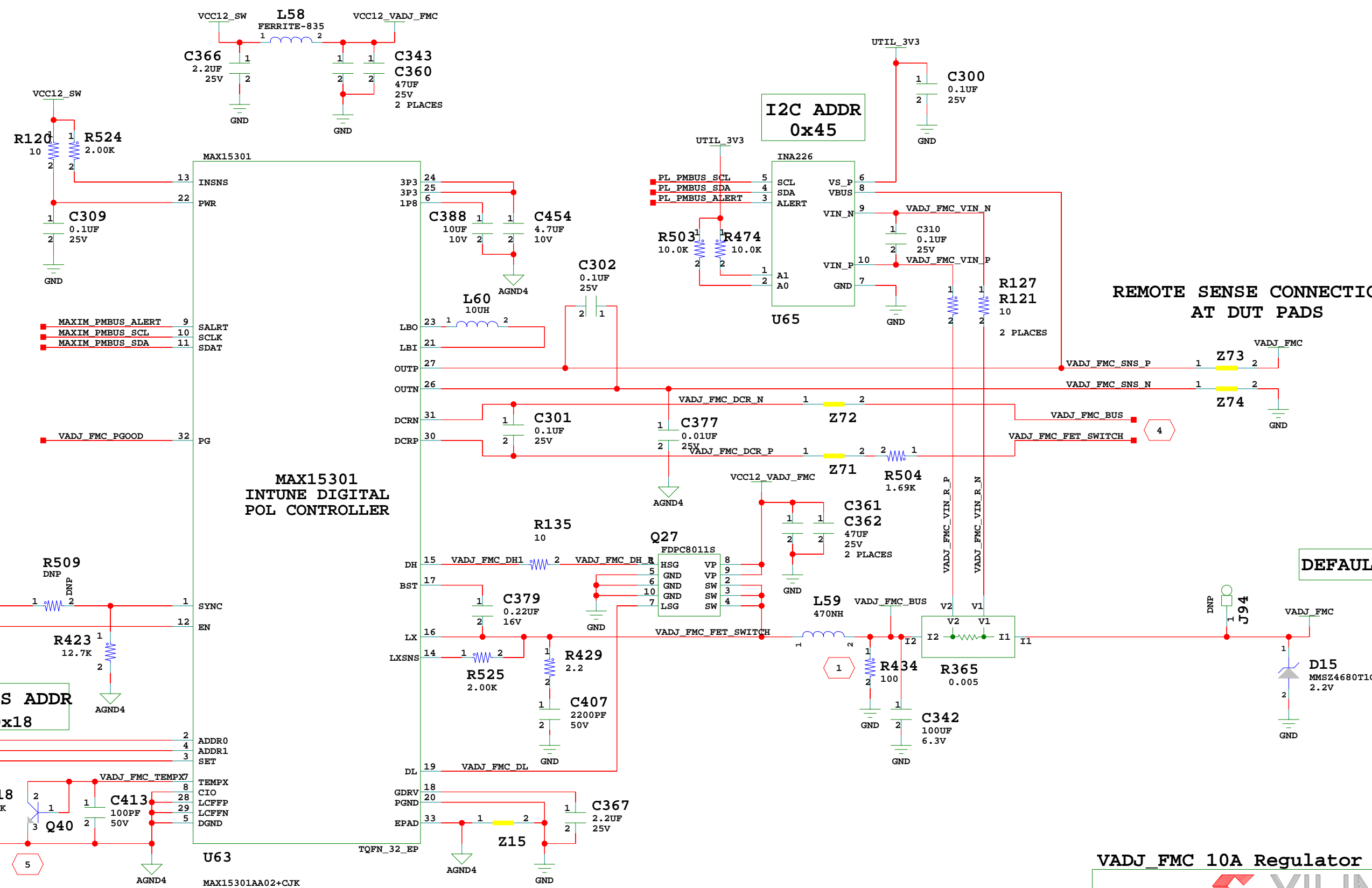


TITLE: VCC3V3 5A Regulator
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU102_REV1_0

ASSY P/N: 0431959
PCB P/N: 1280868
SCH P/N: 0381701
TEST P/N: TSS0179

DATE: 09/20/2016:10:27	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 64 OF 87	DRAWN BY: BF

- 5 PLACE TEMP COMPENSATION TRANSISTOR ON THE BACKSIDE OF THE BOARD DIRECTLY UNDER OUTPUT INDUCTOR
- 4 CONNECT ACROSS PINS OF OUTPUT INDUCTOR
- 3 STRAP RESISTOR ON ADDR1 SETS IOUT_CAL_GAIN (ILIM) TO 2 mOHMS. THIS PARAMETER MUST BE OVERRIDDEN TO 5 mOHMS (MATCHING THE CURRENT SENSE RESISTOR) WHEN THE CONTROLLER IS CONFIGURED.
- 2 HEADER IS FOR SCOPE ATTACHMENT TO OBSERVE STEP LOAD RESPONSE.
- 1 MINIMUM 1K LOAD REQUIRED. MUST BE CONNECTED BEFORE SENSE RESISTOR TO AVOID CONTRIBUTION TO CURRENT MEASUREMENTS.
- 6 TWO VOLTAGE SENSE POINTS ARE REQUIRED DUE TO THE SHAPE AND SIZE OF THE VCC3V3 PLANE.



REMOTE SENSE CONNECTIONS
AT DUT PADS

DEFAULT = 1.80V

VADJ_FMC 10A Regulator



TITLE: VADJ_FMC 10A Regulator SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
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DATE: 09/20/2016:10:27	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 65 OF 87	DRAWN BY: BF

- 5 PLACE TEMP COMPENSATION TRANSISTOR ON THE BACKSIDE OF THE BOARD DIRECTLY UNDER INDUCTOR L3
- 4 CONNECT ACROSS PINS OF OUTPUT INDUCTOR
- 3 STRAP RESISTOR ON ADDR1 SETS IOUT_CAL_GAIN (ILIM) TO 2 mOHMS. THIS PARAMETER MUST BE OVERRIDDEN TO 5 mOHMS (MATCHING THE CURRENT SENSE RESISTOR) WHEN THE CONTROLLER IS CONFIGURED.
- 2 HEADER IS FOR SCOPE ATTACHMENT TO OBSERVE STEP LOAD RESPONSE.
- 1 MINIMUM 1K LOAD REQUIRED. MUST BE CONNECTED BEFORE SENSE RESISTOR TO AVOID CONTRIBUTION TO CURRENT MEASUREMENTS.

NOTES

- 1 Capacitors should be placed as close as possible to Pin12 and 14

SPLIT POWER PLANE REMOTE SENSE CONNECTIONS AT DUT PADS

DEFAULT = 0.90VDC

MGTAVCC 6A Regulator



TITLE: MGTAVCC 6A Regulator
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU102_REV1_0

ASSY P/N: 0431959
PCB P/N: 1280868
SCH P/N: 0381701
TEST P/N: TSS0179

DATE: 09/20/2016:10:26

VER: 1.0

SHEET SIZE: B

REV: 01

SHEET

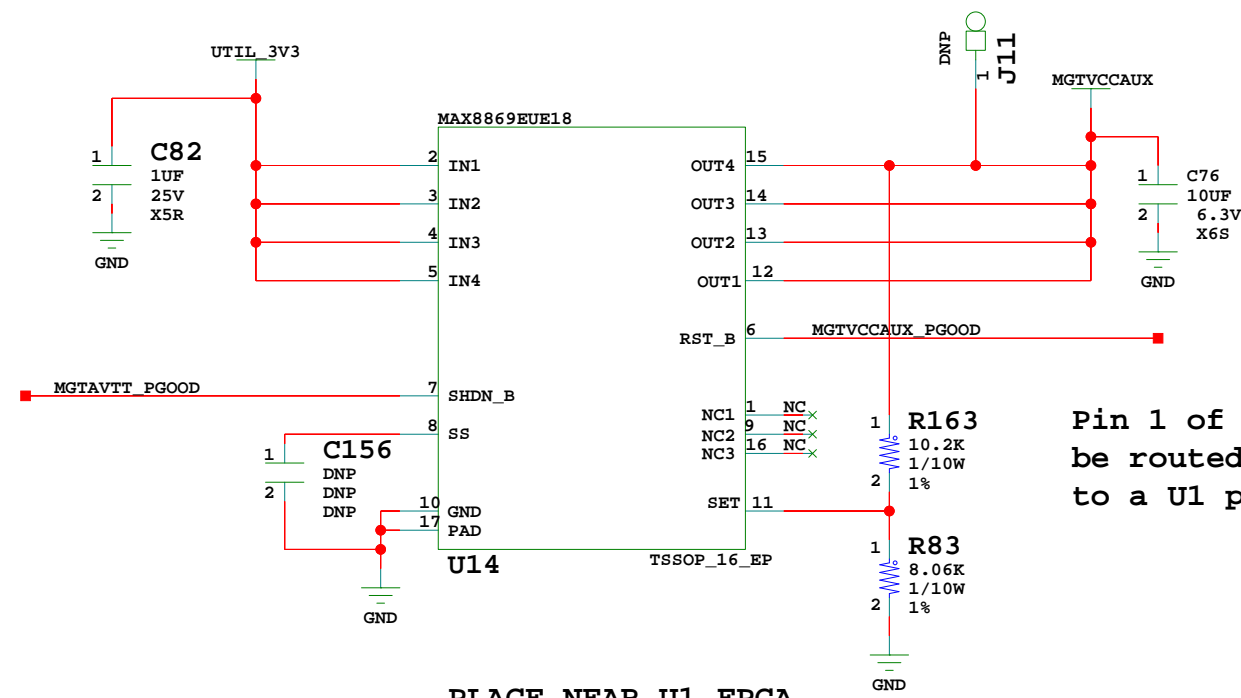
OF

67

87

DRAWN BY:

BF




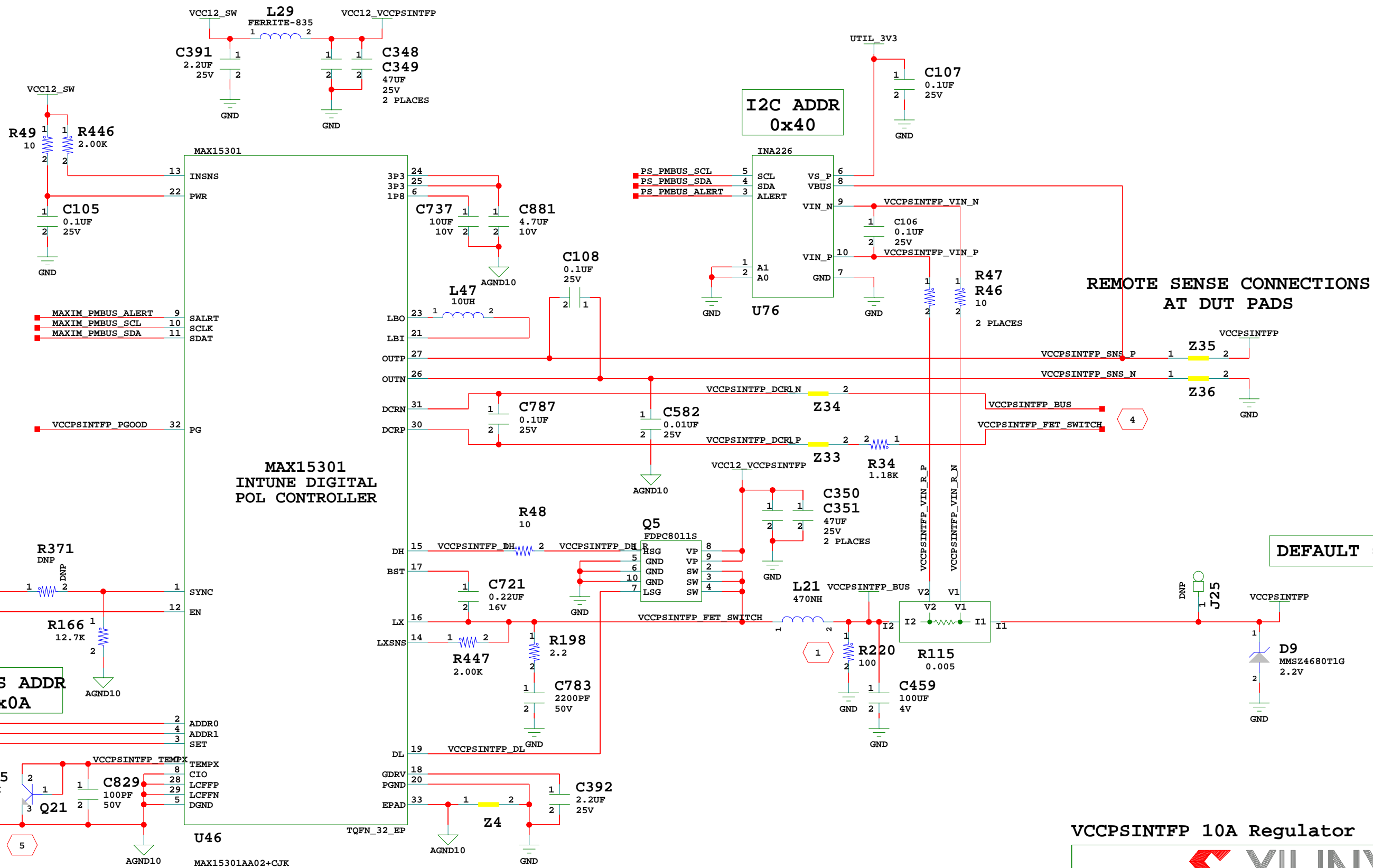
PLACE NEAR U1 FPGA

Pin 1 of 10.2K resistor must be routed as a sense line directly to a U1 power pin

DEFAULT = 1.81VDC

MGTVCCAUX 1A Regulator

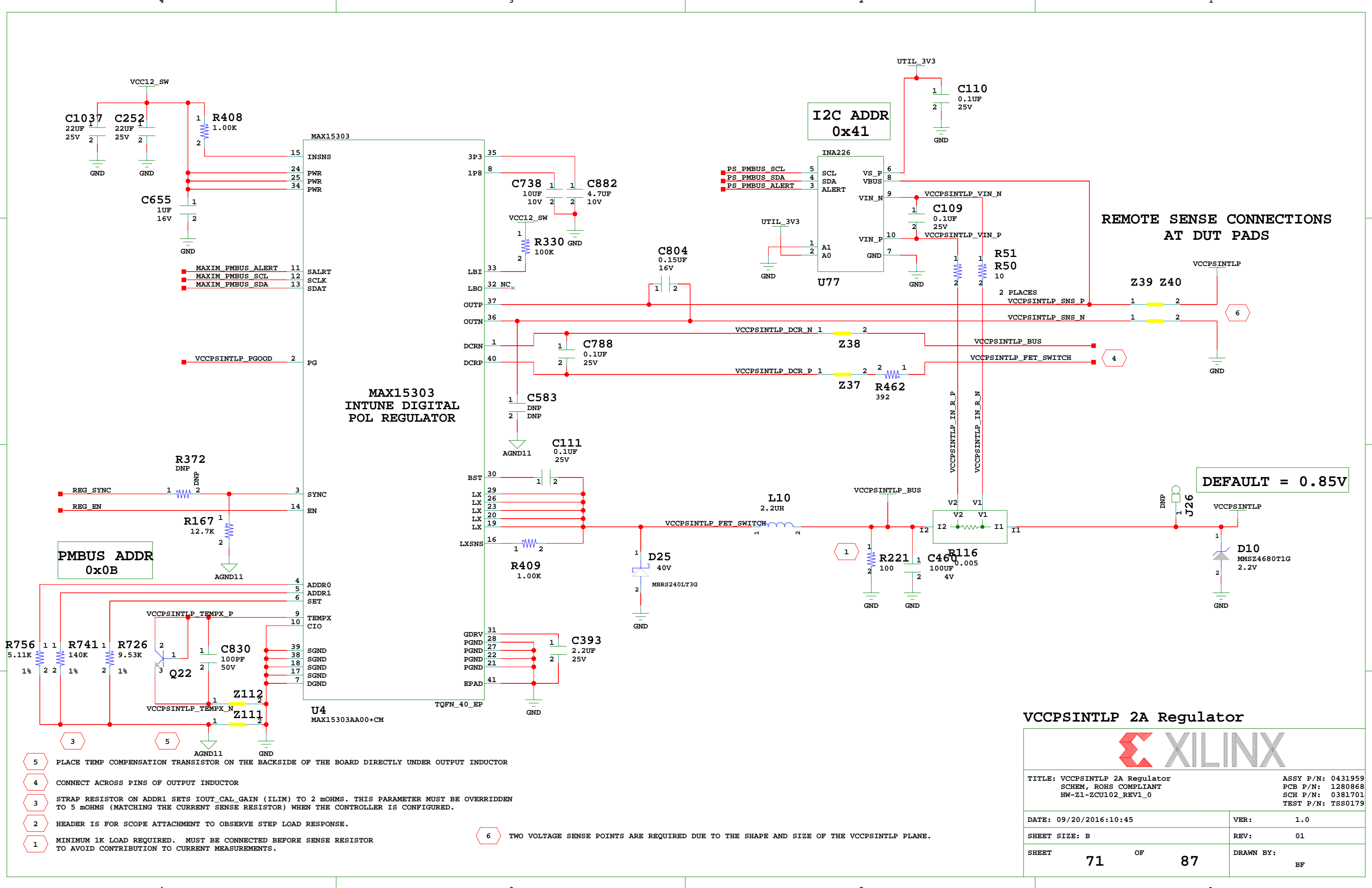
	
TITLE: MGTVCCAUX 1A Regulator SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	
ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179	
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 69 OF 87	DRAWN BY: BF



- 5 PLACE TEMP COMPENSATION TRANSISTOR ON THE BACKSIDE OF THE BOARD DIRECTLY UNDER INDUCTOR L3
- 4 CONNECT ACROSS PINS OF INDUCTOR L3
- 3 STRAP RESISTOR ON ADDR1 SETS IOUT_CAL_GAIN (ILIM) TO 2 MOHMS. THIS PARAMETER MUST BE OVERRIDDEN TO 5 MOHMS (MATCHING THE CURRENT SENSE RESISTOR) WHEN THE CONTROLLER IS CONFIGURED.
- 2 HEADER IS FOR SCOPE ATTACHMENT TO OBSERVE STEP LOAD RESPONSE.
- 1 MINIMUM 1K LOAD REQUIRED. MUST BE CONNECTED BEFORE SENSE RESISTOR TO AVOID CONTRIBUTION TO CURRENT MEASUREMENTS.

VCCPSINTFP 10A Regulator

TITLE: VCCPSINTFP 10A Regulator SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	
ASSY P/N: 0431809 PCB P/N: 1280819 SCH P/N: 0381582 TEST P/N: TSS0164	
DATE: 09/20/2016:10:26	VER: A.0
SHEET SIZE: B	REV: 01
SHEET 70 OF 87	DRAWN BY: RN

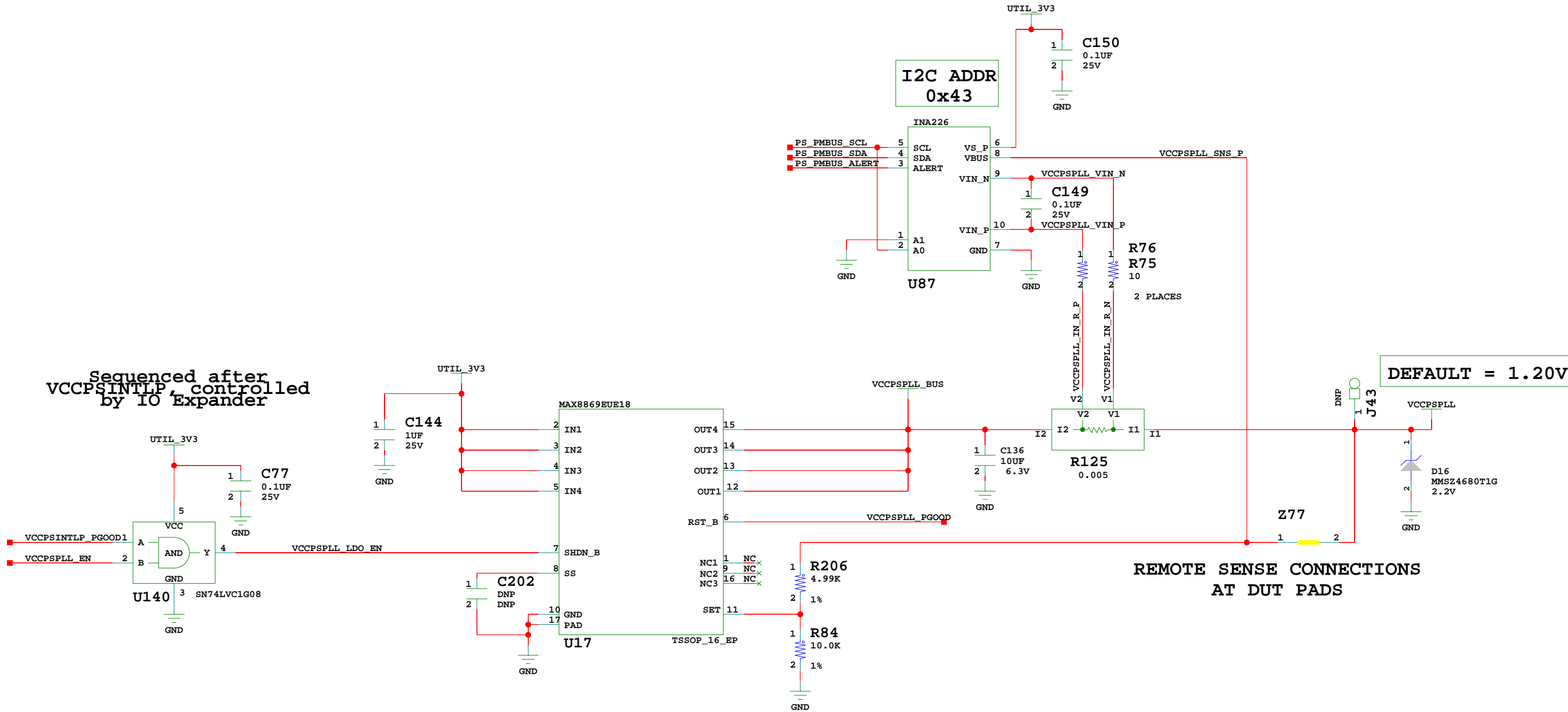


- 5 PLACE TEMP COMPENSATION TRANSISTOR ON THE BACKSIDE OF THE BOARD DIRECTLY UNDER OUTPUT INDUCTOR
- 4 CONNECT ACROSS PINS OF OUTPUT INDUCTOR
- 3 STRAP RESISTOR ON ADDR1 SETS IOUT_CAL_GAIN (ILIM) TO 2 MOHMS. THIS PARAMETER MUST BE OVERRIDDEN TO 5 MOHMS (MATCHING THE CURRENT SENSE RESISTOR) WHEN THE CONTROLLER IS CONFIGURED.
- 2 HEADER IS FOR SCOPE ATTACHMENT TO OBSERVE STEP LOAD RESPONSE.
- 1 MINIMUM 1K LOAD REQUIRED. MUST BE CONNECTED BEFORE SENSE RESISTOR TO AVOID CONTRIBUTION TO CURRENT MEASUREMENTS.


6 TWO VOLTAGE SENSE POINTS ARE REQUIRED DUE TO THE SHAPE AND SIZE OF THE VCCPSINTLP PLANE.

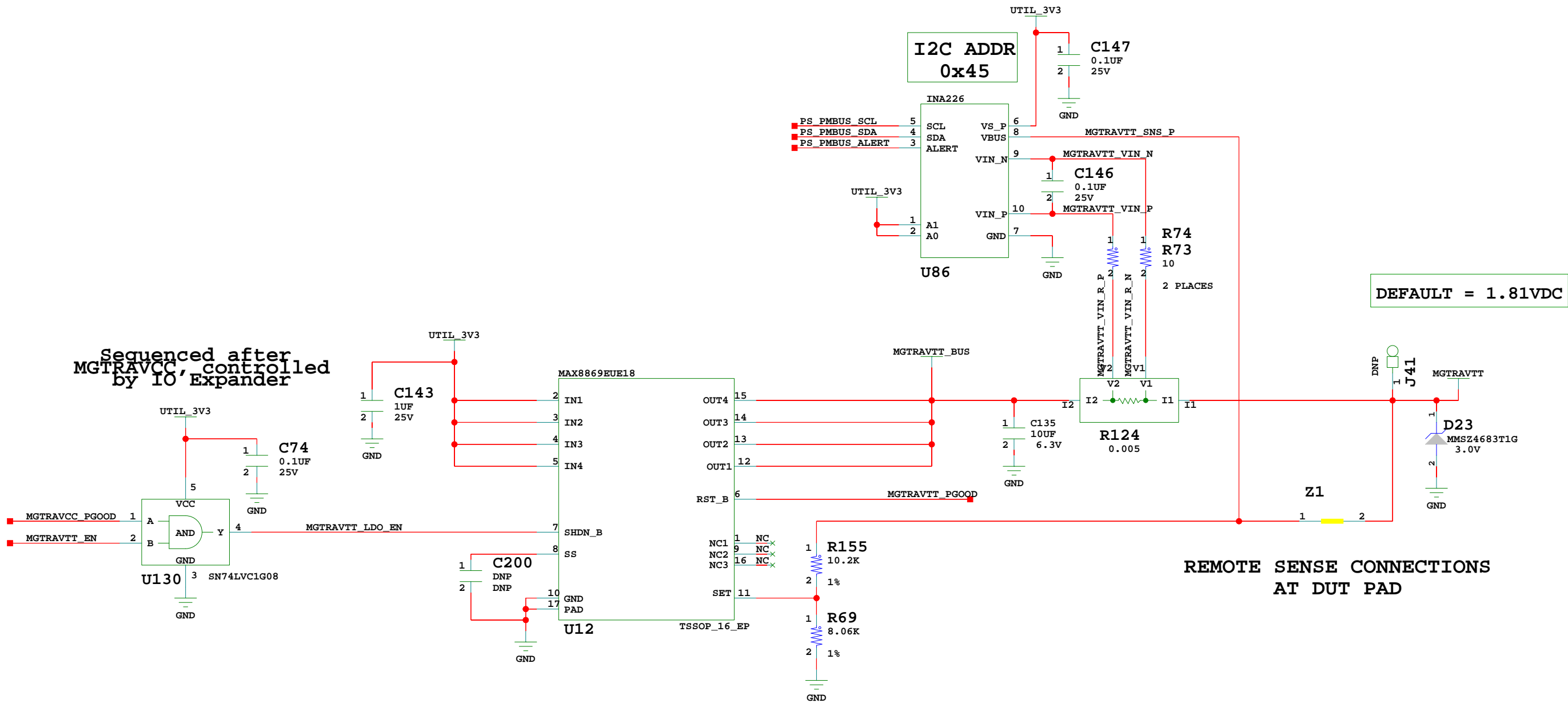
VCCPSINTLP 2A Regulator

TITLE: VCCPSINTLP 2A Regulator SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	
ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179	
DATE: 09/20/2016:10:45	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 71 OF 87	DRAWN BY: BF



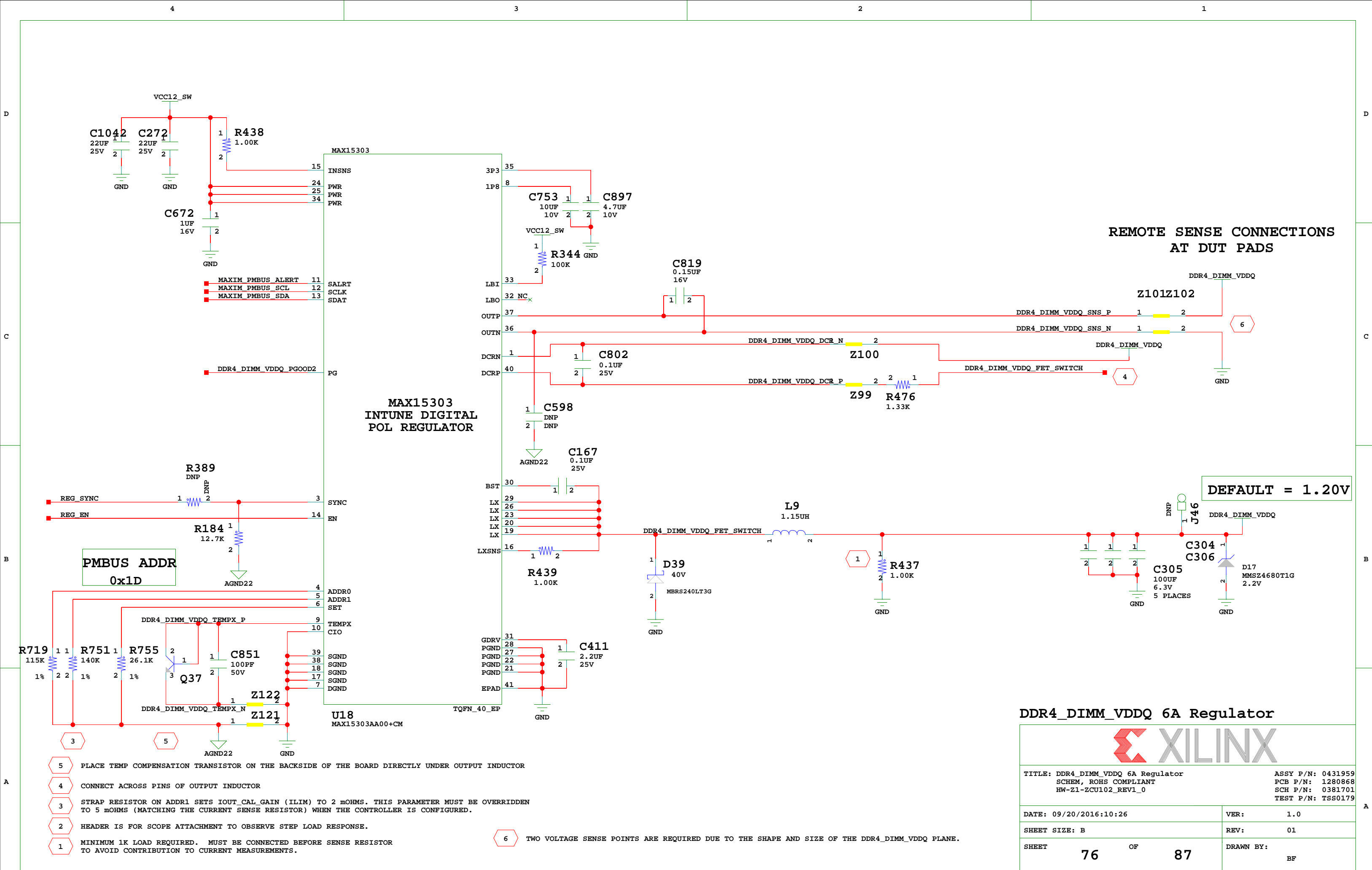
VCCPSPLL 200MA Regulator

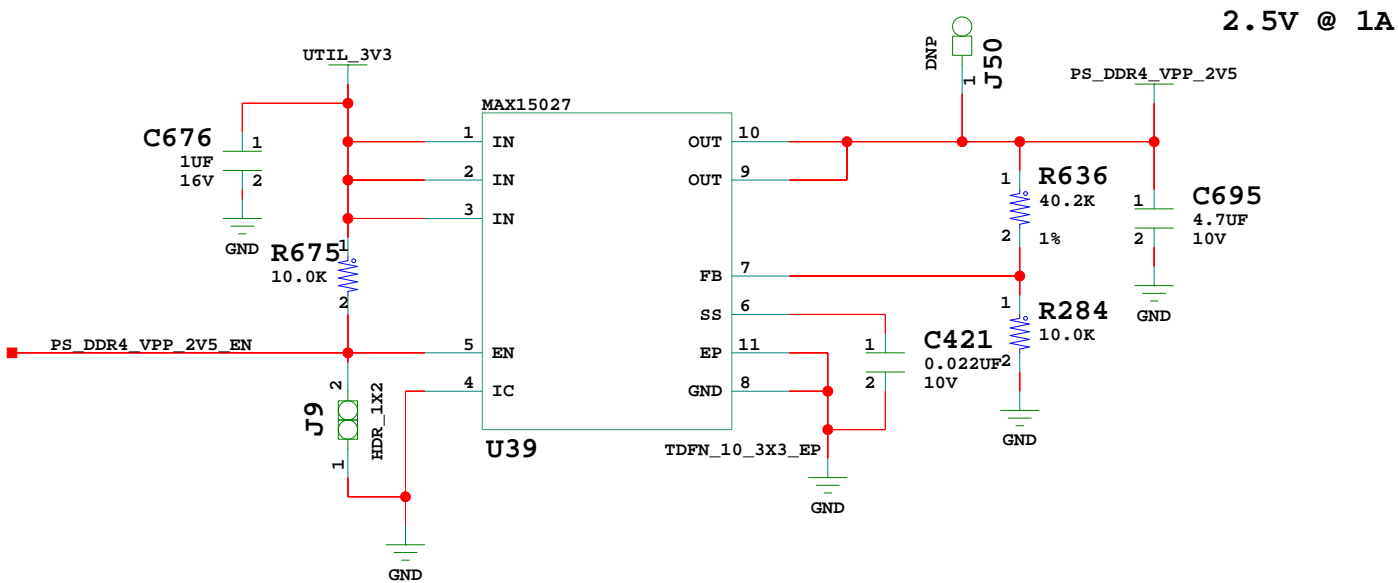
	
TITLE: VCCPSPLL 200MA Regulator SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	
ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179	
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 73 OF 87	DRAWN BY: BF



MGTRAVTT 100MA Regulator

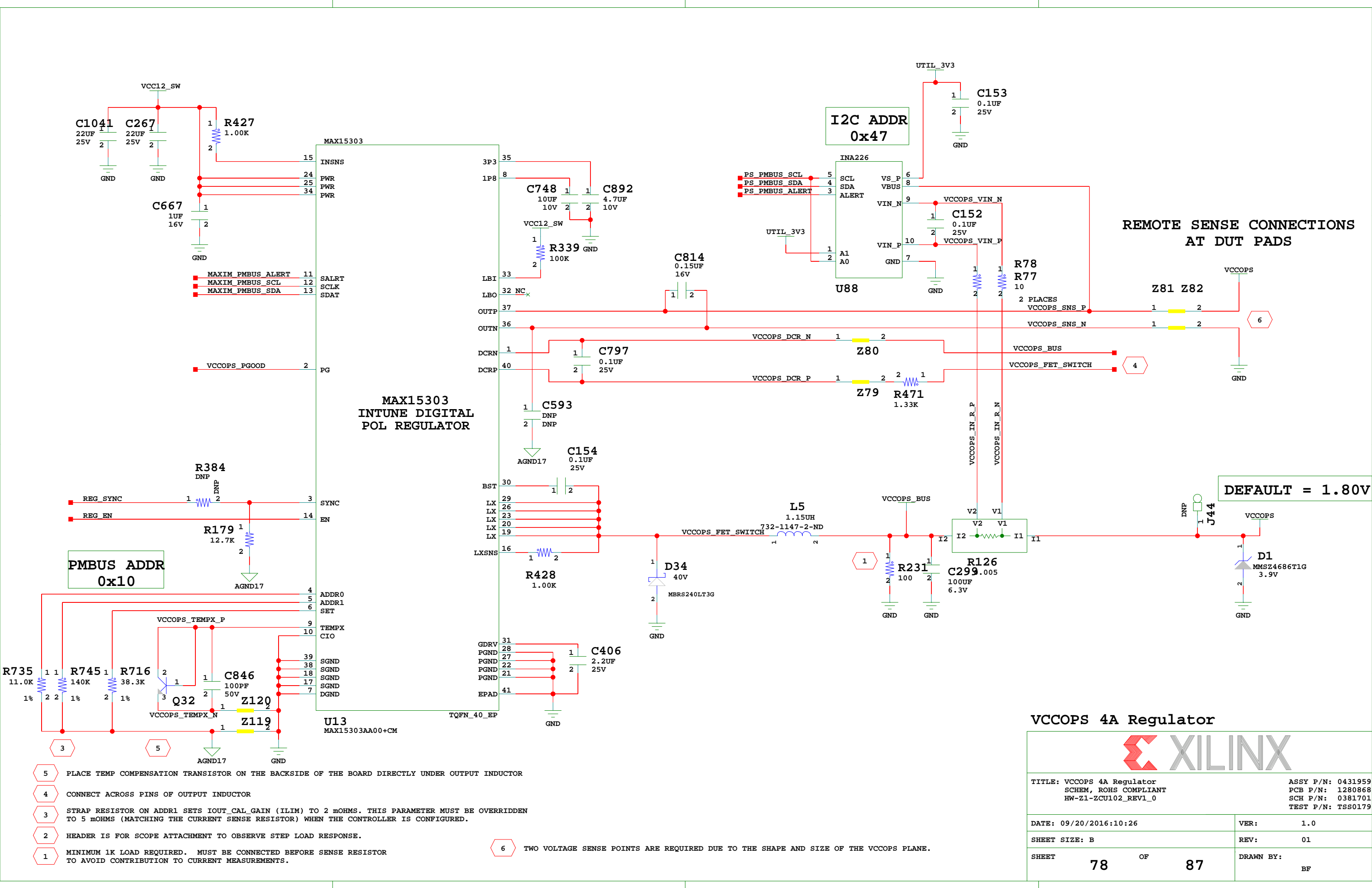
TITLE: MGTRAVTT 100MA Regulator SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	
ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179	
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 75 OF 87	DRAWN BY: BF





PS_DDR4_VPP_2V5 1A Regulator

TITLE: PS_DDR4_VPP_2V5 1A Regulator		ASSY P/N: 0431959	
SCHEM, ROHS COMPLIANT		PCB P/N: 1280868	
HW-Z1-ZCU102_REV1_0		SCH P/N: 0381701	
		TEST P/N: TSS0179	
DATE: 09/20/2016:10:26		VER:	1.0
SHEET SIZE: B		REV:	01
SHEET	77	OF	87
		DRAWN BY:	BF

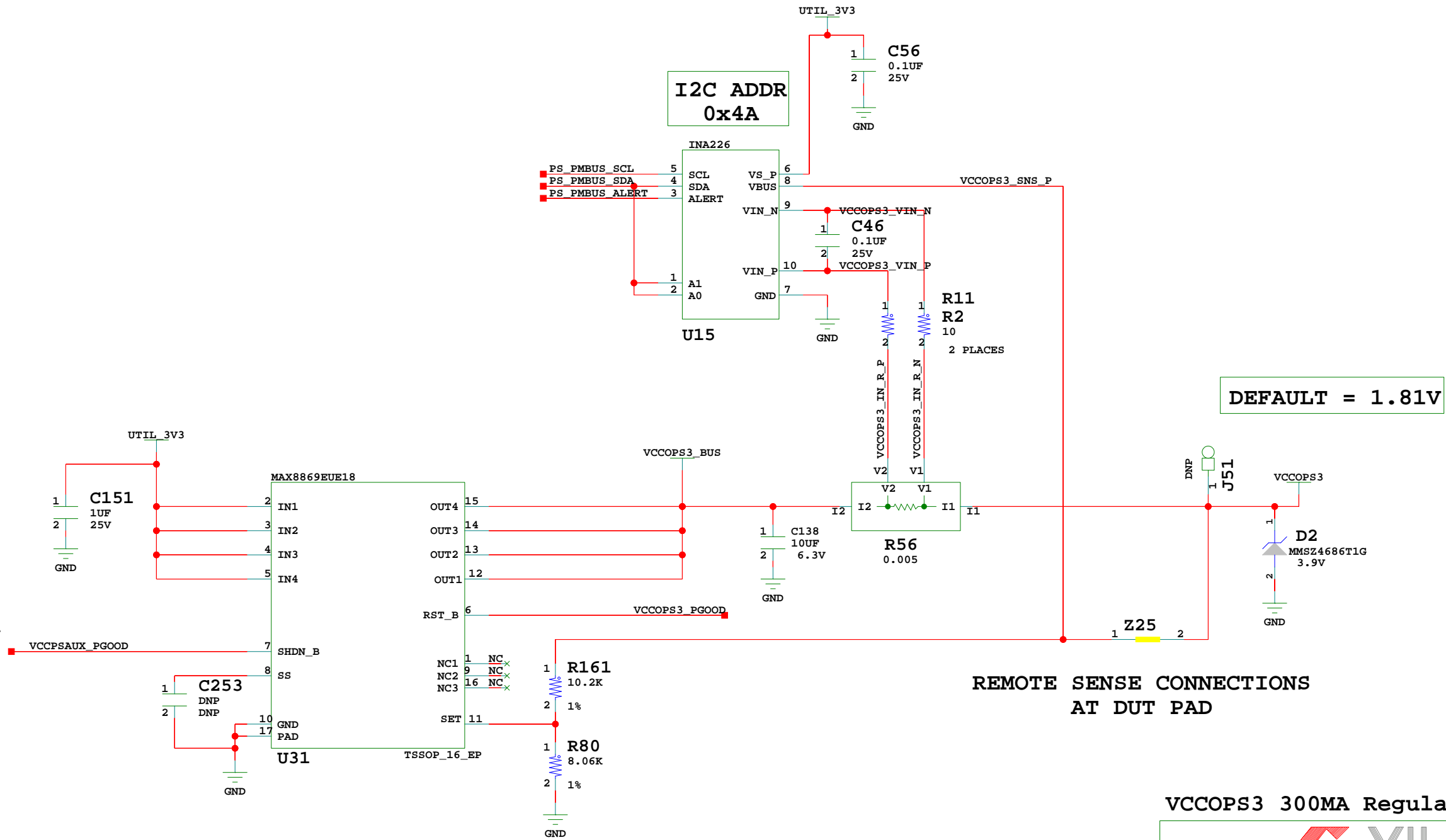


- 5 PLACE TEMP COMPENSATION TRANSISTOR ON THE BACKSIDE OF THE BOARD DIRECTLY UNDER OUTPUT INDUCTOR
- 4 CONNECT ACROSS PINS OF OUTPUT INDUCTOR
- 3 STRAP RESISTOR ON ADDR1 SETS IOUT_CAL_GAIN (ILIM) TO 2 mOHMS. THIS PARAMETER MUST BE OVERRIDDEN TO 5 mOHMS (MATCHING THE CURRENT SENSE RESISTOR) WHEN THE CONTROLLER IS CONFIGURED.
- 2 HEADER IS FOR SCOPE ATTACHMENT TO OBSERVE STEP LOAD RESPONSE.
- 1 MINIMUM 1K LOAD REQUIRED. MUST BE CONNECTED BEFORE SENSE RESISTOR TO AVOID CONTRIBUTION TO CURRENT MEASUREMENTS.
- 6 TWO VOLTAGE SENSE POINTS ARE REQUIRED DUE TO THE SHAPE AND SIZE OF THE VCCOPS PLANE.

VCCOPS 4A Regulator

TITLE: VCCOPS 4A Regulator SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0		ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179	
DATE: 09/20/2016:10:26		VER: 1.0	
SHEET SIZE: B		REV: 01	
SHEET 78 OF 87		DRAWN BY: BF	

Sequenced after
VCCPSAUX

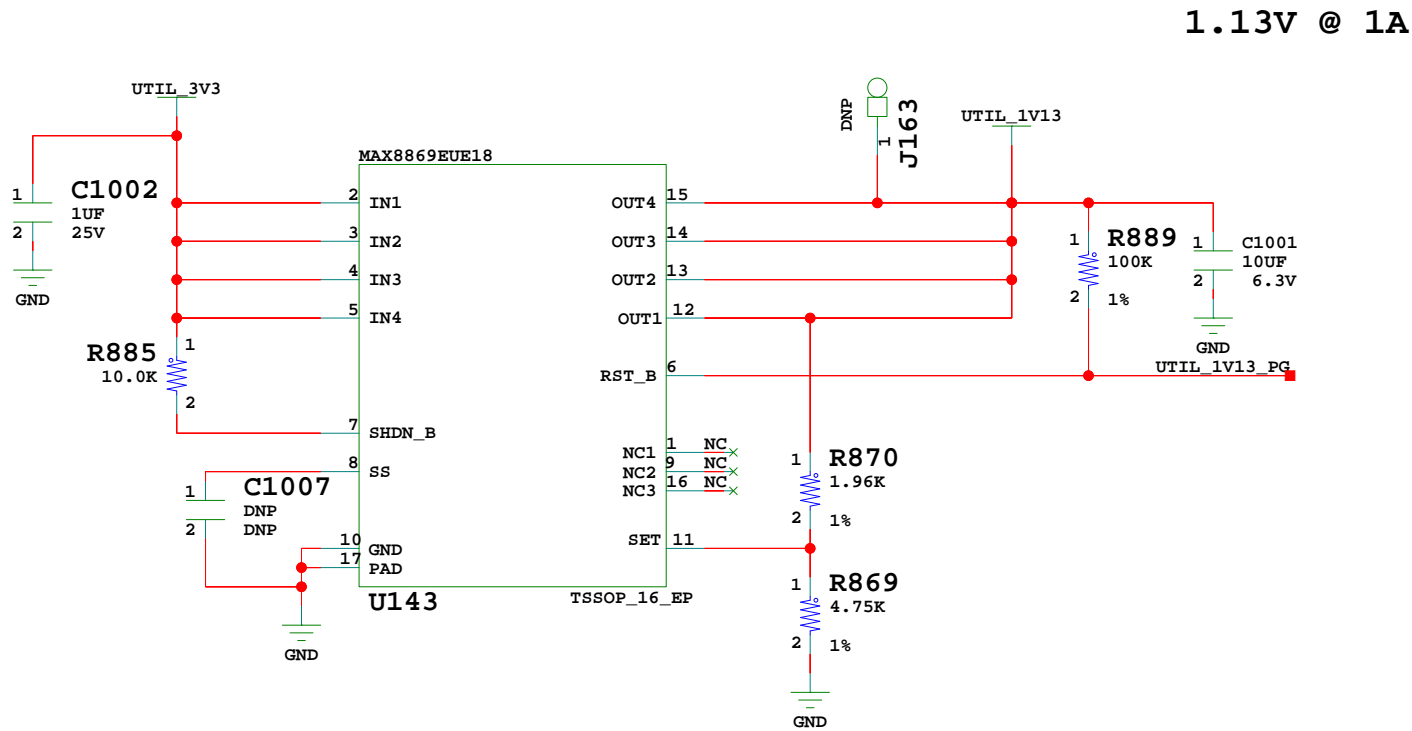


VCCOPS3 300MA Regulator



TITLE: VCCOPS3 300MA Regulator
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU102_REV1_0
ASSY P/N: 0431959
PCB P/N: 1280868
SCH P/N: 0381701
TEST P/N: TSS0179

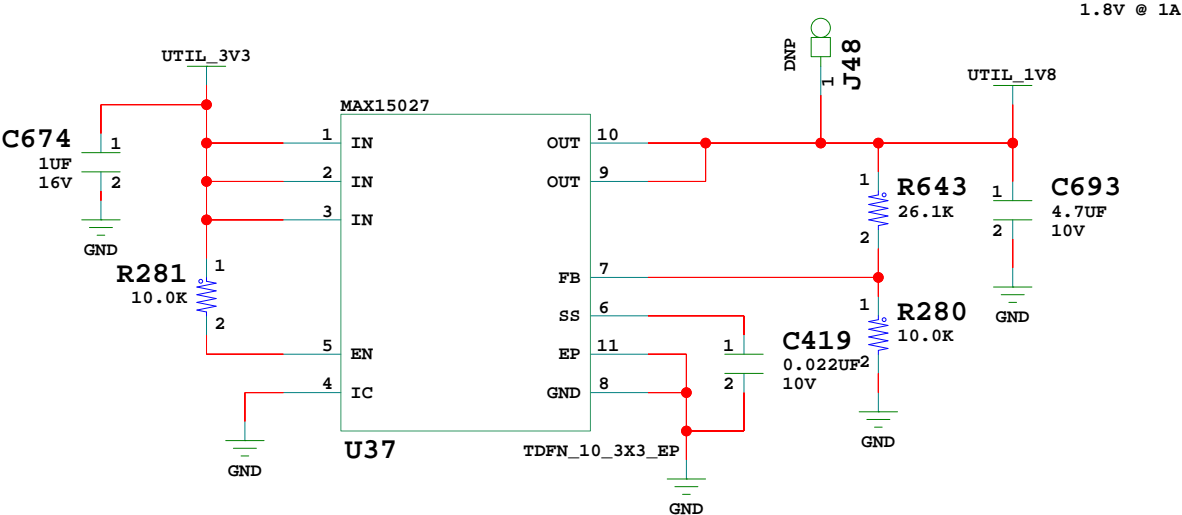
DATE: 09/20/2016:10:27	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 79 OF 87	DRAWN BY: BF



1.13V @ 1A satisfies voltage and total current requirements for TI ENET PHY, as well as HDMI TX and RX transcievers

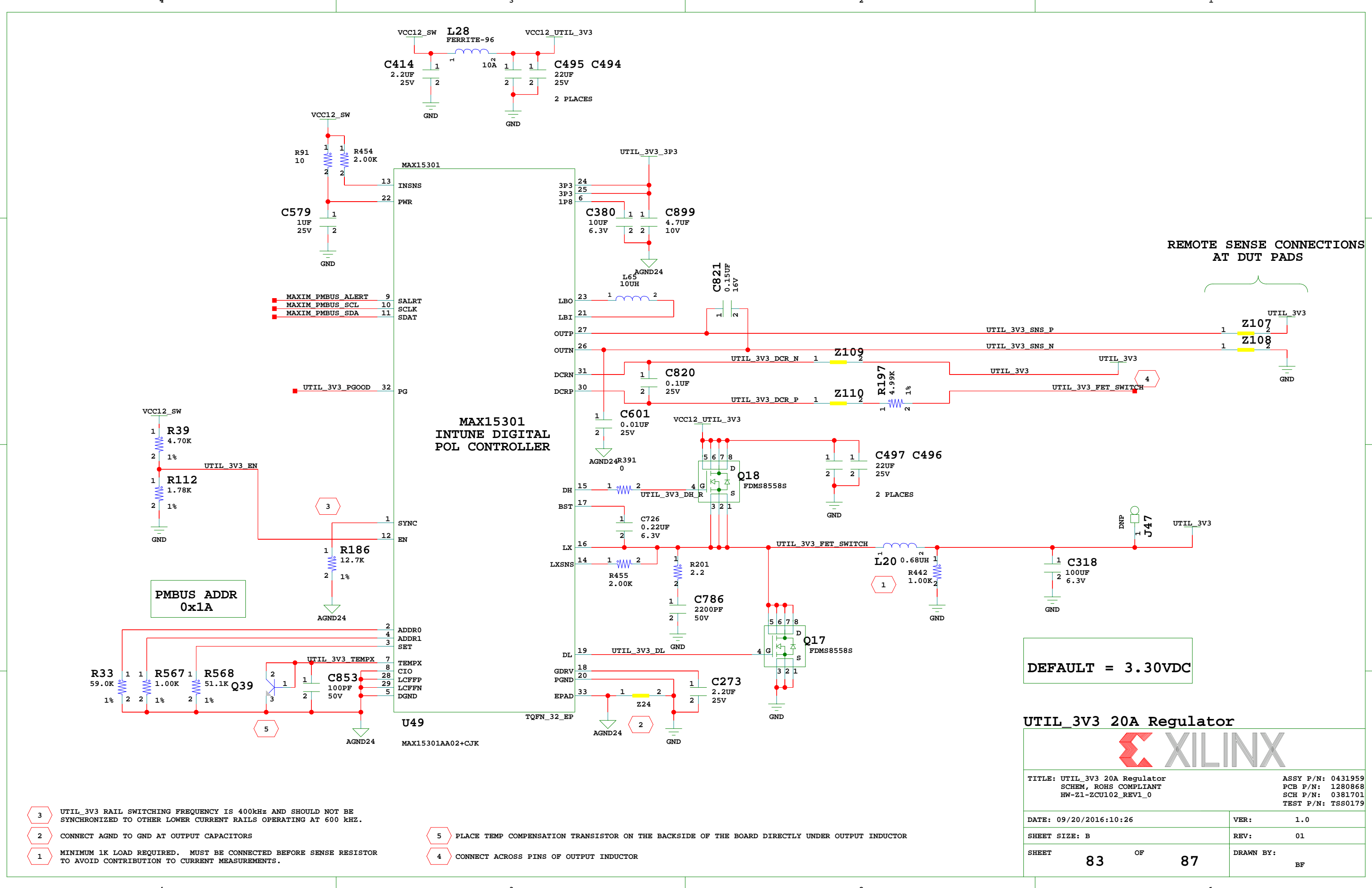
UTIL_1V13 1A Regulator

TITLE: UTIL_1V13 1A Regulator SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0		ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179	
DATE: 09/20/2016:10:27		VER:	1.0
SHEET SIZE: B		REV:	01
SHEET	81	OF	87
DRAWN BY:		BF	



UTIL_1V8 1A Regulator

TITLE: UTIL_1V8 1A Regulator SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0		ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179	
DATE: 09/20/2016:10:26		VER:	1.0
SHEET SIZE: B		REV:	01
SHEET	82 OF 87	DRAWN BY:	BF



- 3

UTIL_3V3 RAIL SWITCHING FREQUENCY IS 400kHz AND SHOULD NOT BE SYNCHRONIZED TO OTHER LOWER CURRENT RAILS OPERATING AT 600 KHZ.
- 2

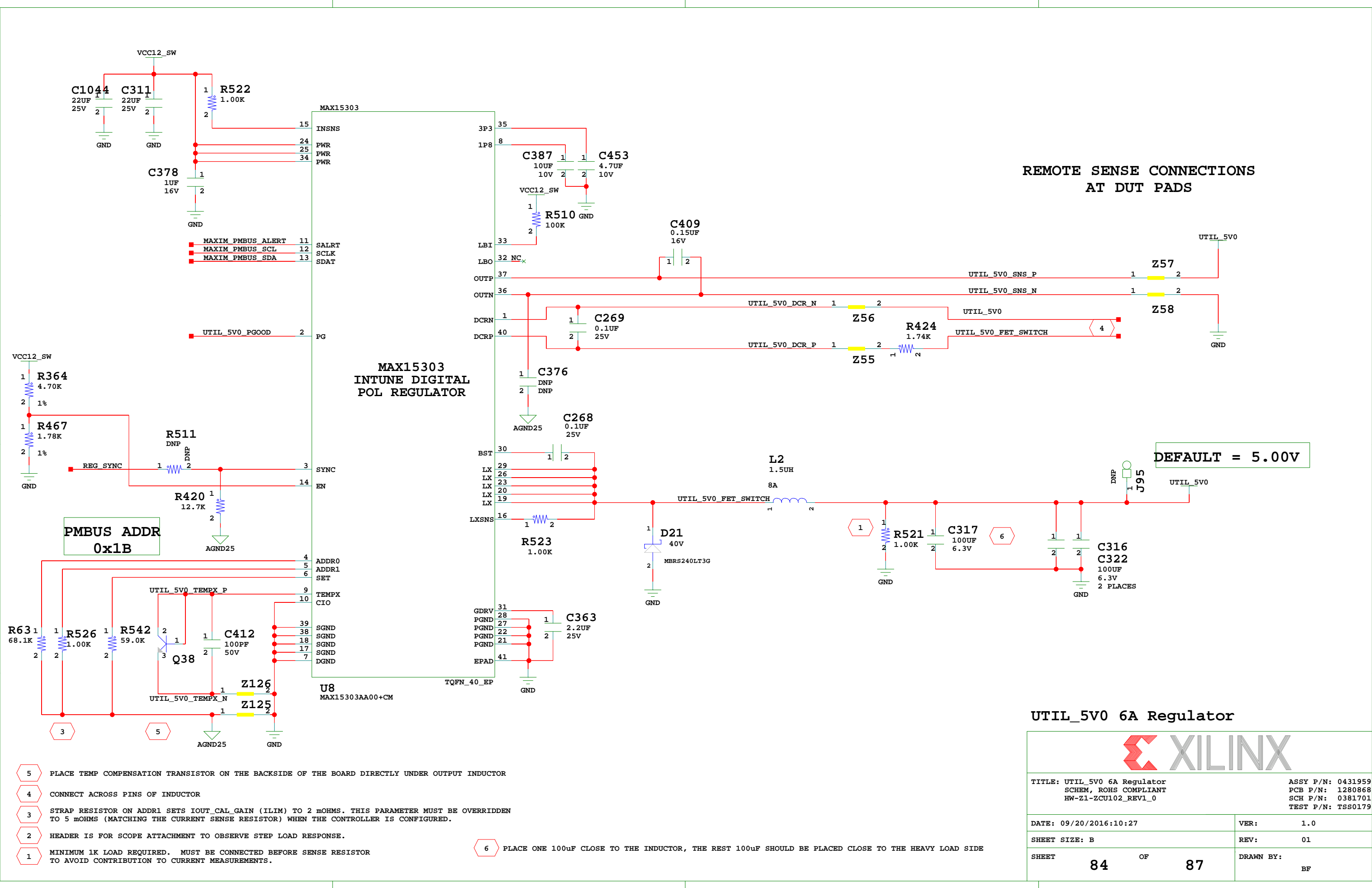
CONNECT AGND TO GND AT OUTPUT CAPACITORS
- 1

MINIMUM 1K LOAD REQUIRED. MUST BE CONNECTED BEFORE SENSE RESISTOR TO AVOID CONTRIBUTION TO CURRENT MEASUREMENTS.
- 5

PLACE TEMP COMPENSATION TRANSISTOR ON THE BACKSIDE OF THE BOARD DIRECTLY UNDER OUTPUT INDUCTOR
- 4

CONNECT ACROSS PINS OF OUTPUT INDUCTOR

<div><div></div><div>XILINX</div></div>	
TITLE: UTIL_3V3 20A Regulator SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 83 OF 87	DRAWN BY: BF



MAX15303
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POL REGULATOR

REMOTE SENSE CONNECTIONS
AT DUT PADS

DEFAULT = 5.00V

UTIL_5V0 6A Regulator

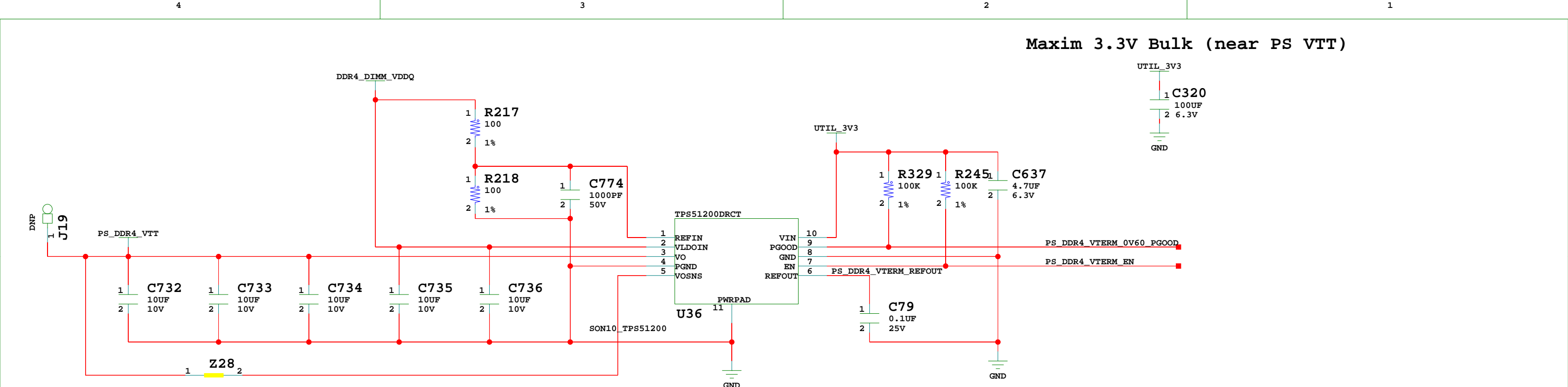


TITLE: UTIL_5V0 6A Regulator
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU102_REV1_0

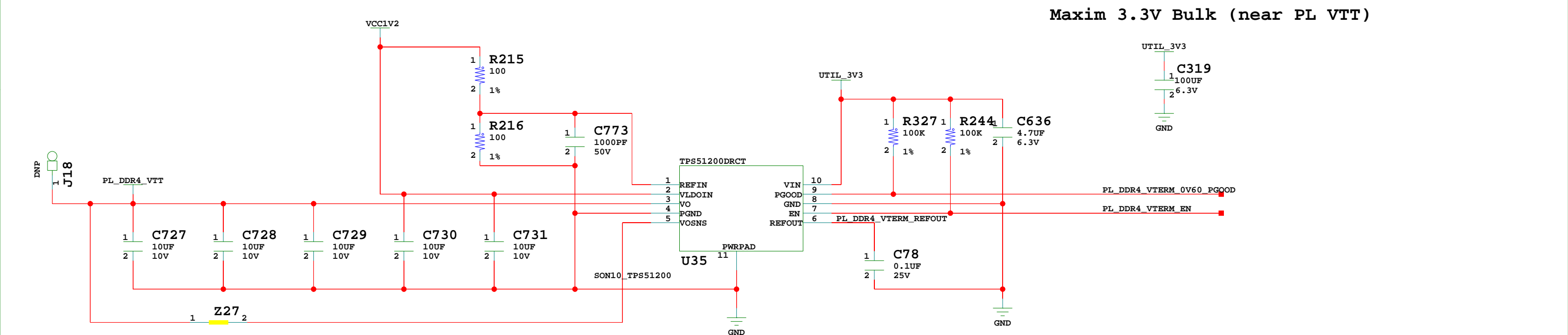
ASSY P/N: 0431959
PCB P/N: 1280868
SCH P/N: 0381701
TEST P/N: TSS0179

DATE: 09/20/2016:10:27	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 84 OF 87	DRAWN BY: BF

- 5 PLACE TEMP COMPENSATION TRANSISTOR ON THE BACKSIDE OF THE BOARD DIRECTLY UNDER OUTPUT INDUCTOR
- 4 CONNECT ACROSS PINS OF INDUCTOR
- 3 STRAP RESISTOR ON ADDR1 SETS IOUT_CAL_GAIN (ILIM) TO 2 mOHMS. THIS PARAMETER MUST BE OVERRIDDEN TO 5 mOHMS (MATCHING THE CURRENT SENSE RESISTOR) WHEN THE CONTROLLER IS CONFIGURED.
- 2 HEADER IS FOR SCOPE ATTACHMENT TO OBSERVE STEP LOAD RESPONSE.
- 1 MINIMUM 1K LOAD REQUIRED. MUST BE CONNECTED BEFORE SENSE RESISTOR TO AVOID CONTRIBUTION TO CURRENT MEASUREMENTS.
- 6 PLACE ONE 100uF CLOSE TO THE INDUCTOR, THE REST 100uF SHOULD BE PLACED CLOSE TO THE HEAVY LOAD SIDE



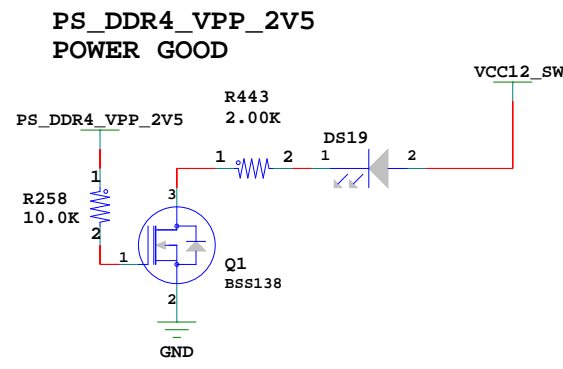
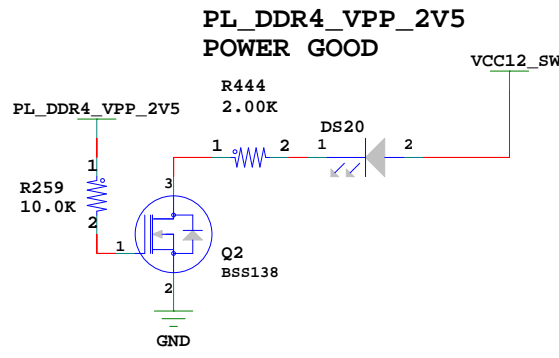
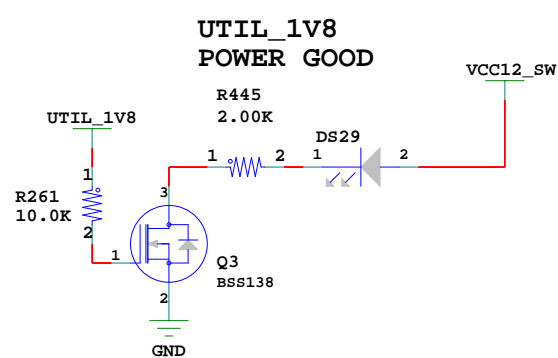
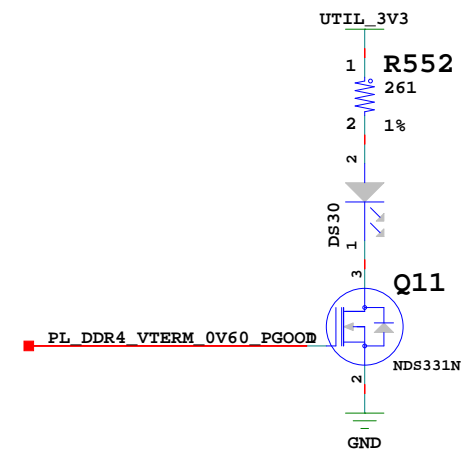
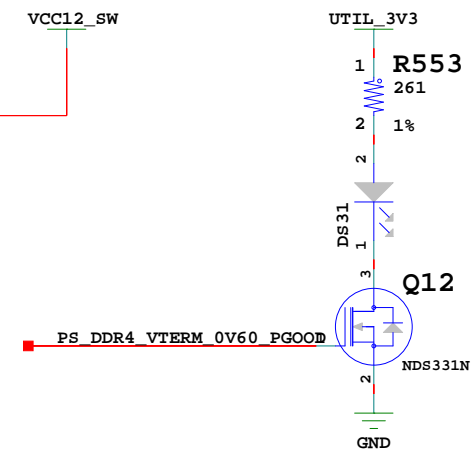
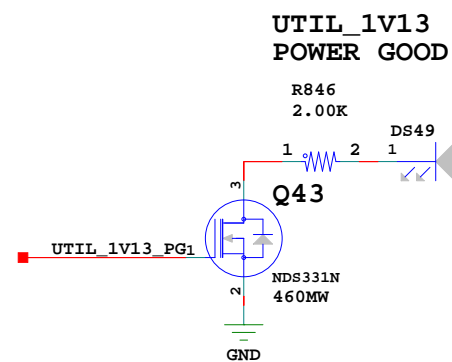
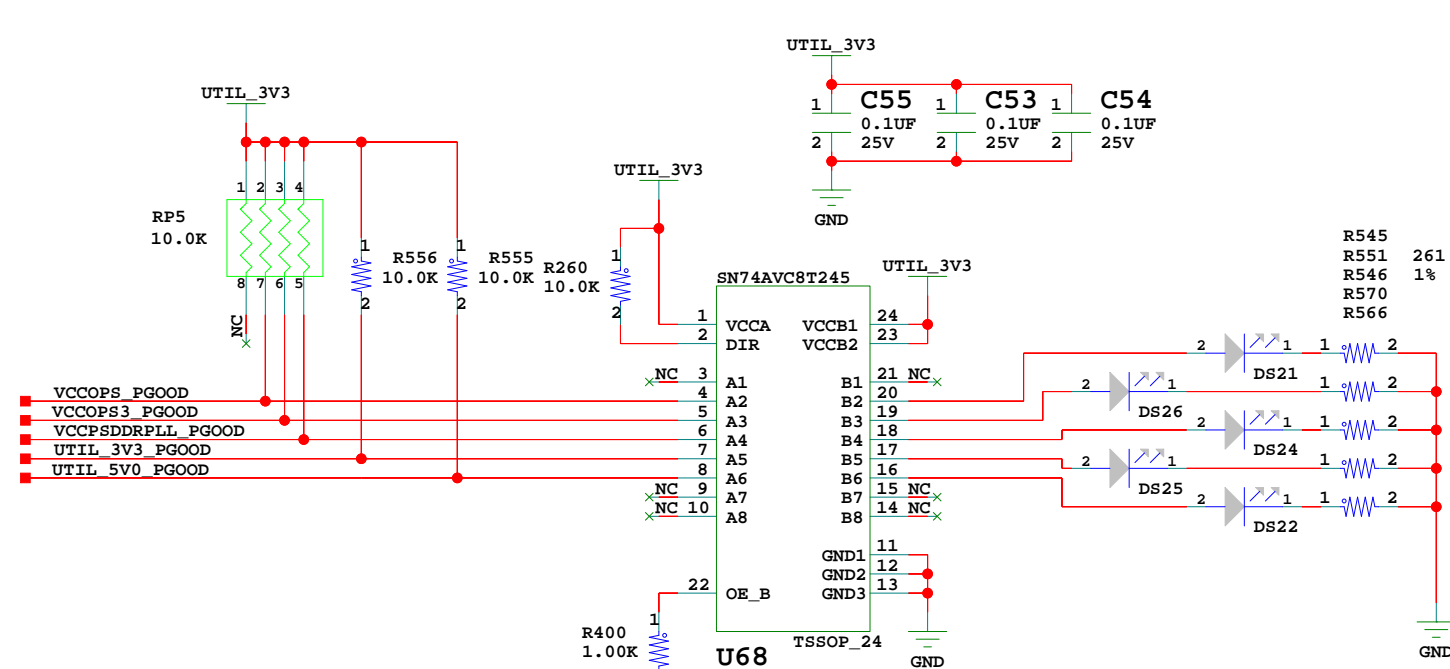
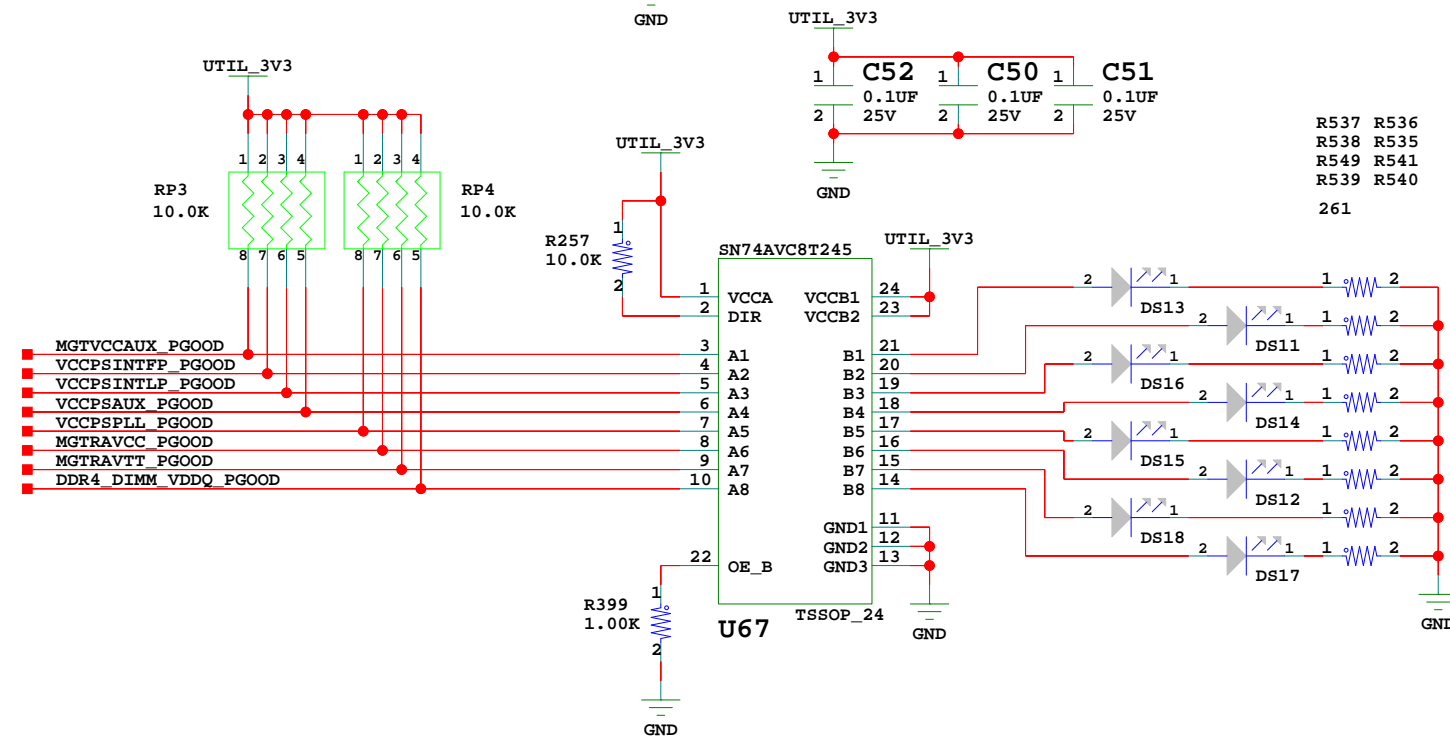
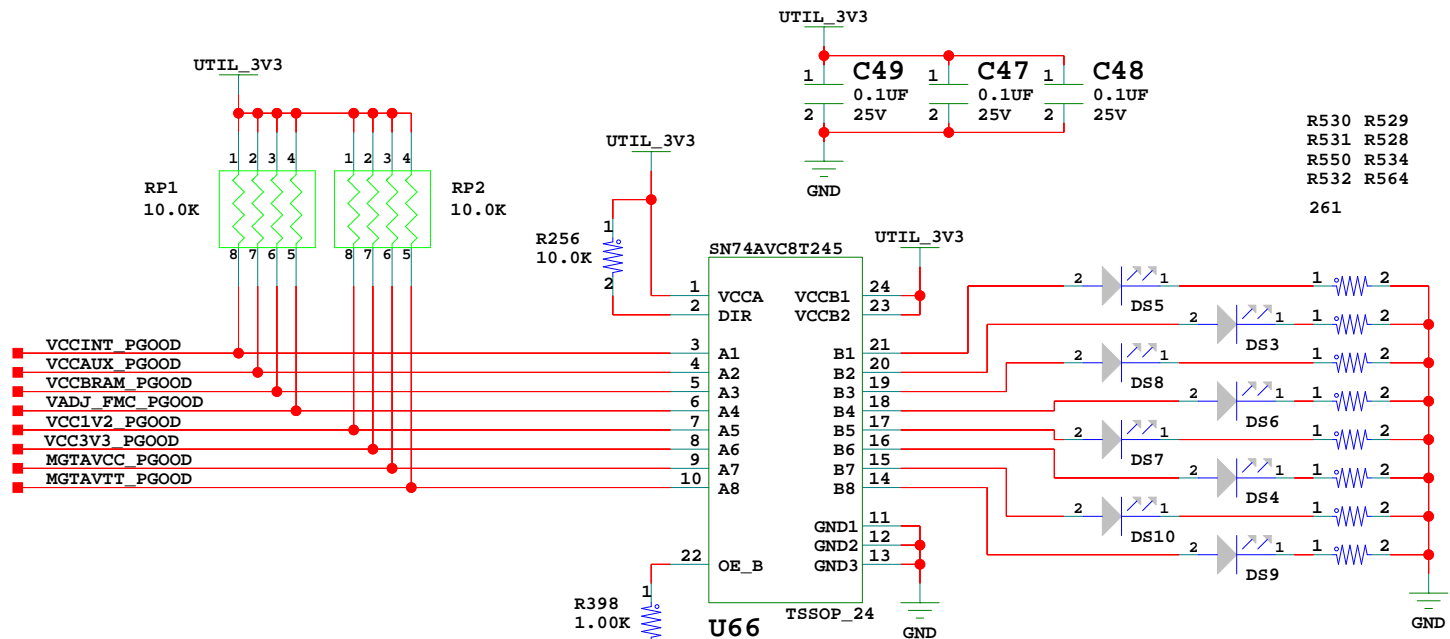
Place sense near DDR4 DIMM



Place sense near DDR4 components

DDR4 Termination Supply

TITLE: DDR4 Termination Supply SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0		ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179	
DATE: 09/20/2016:10:45		VER:	1.0
SHEET SIZE: B		REV:	01
SHEET	85	OF	87
DRAWN BY:		BF	



Power Status LEDs

TITLE: Power Status LEDs SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	
ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179	
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 86 OF 87	DRAWN BY: BF

