

ALIGN: Analog Layout, Intelligently Generated from Netlists

OTA Testbench

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- A testbench is required for performance verification of the designed block
- This document reports the various testbenches required to do performance verification of OTA
- Slide 3 shows the table of testbenches required to be tested in sequence
- Slide 4 shows the schematic view of all testbenches in a table
- A sequence is necessary as other testbenches are dependent on other parameters from DC/AC testbench
- In each testbench, the OTA/design under test (DUT) is tested using technology-independent model (for example, current source, voltage supply, PWL)
- Hence, these testbenches are technology independent and can be used for any OTA designed for any technology
- Steps identified for each testbench can be automated
- Currently these testbenches have been designed for single-ended OTA

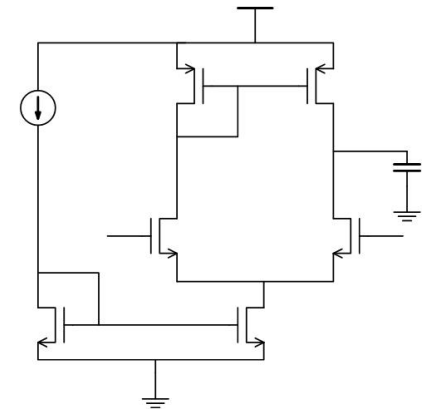


Fig 1. 5T OTA schematic



OTA Testbench

Sequence	OTA Specification	Units
DC-1	ICMR	V
DC-2	OCMR	V
NOISE-1	Input Noise	V^2/Hz
AC-1	DC gain (A_{DC})	dB
	3-dB bandwidth (BW_{3dB})	MHz
	Unity Gain Frequency	MHz
	Phase Margin (PM)	deg
	Gain Margin (GM)	dB
AC-2	Common Mode Rejection Ratio (CMRR)	dB
AC-3	PSRR+	dB
AC-4	PSRR-	dB
TRAN-1	Slew Rate (SR)	V/ μsec

Table 1 : Standard OTA Specifications and their required testbenches



OTA Testbench: Schematic view

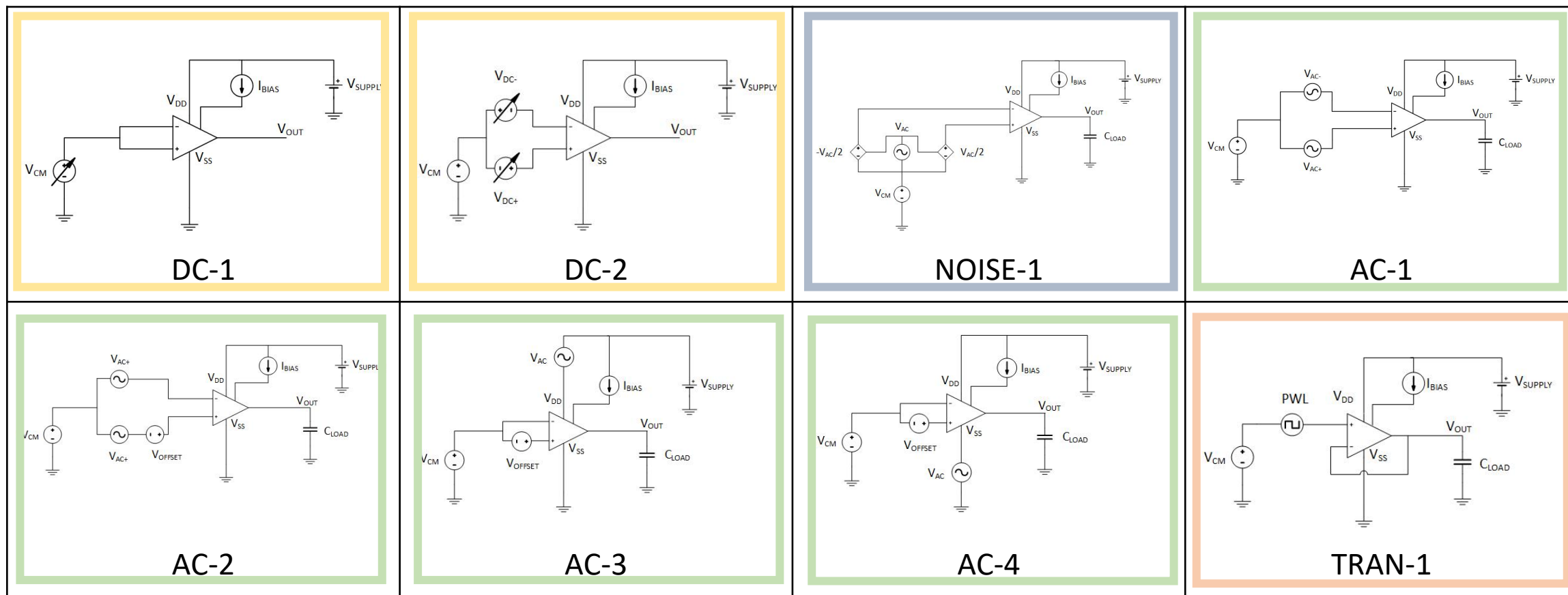


Table 2 : Schematic view of all OTA testbenches

- Steps for DC-1 Simulation testbench
 1. Set DC conditions of current/voltage bias for the OTA by setting voltage for supply and ground
 2. Do a DC voltage sweep (V_{CM}) on input differential pins from 0 to V_{DD}
 3. Probe the operating region of each transistors in OTA for the sweep range
 4. Range during which all transistors are in their expected region (saturation/triode) will be treated as DC operating range
 5. Input common mode range (ICMR) is the input voltage range for which all transistors are in expected region of operation

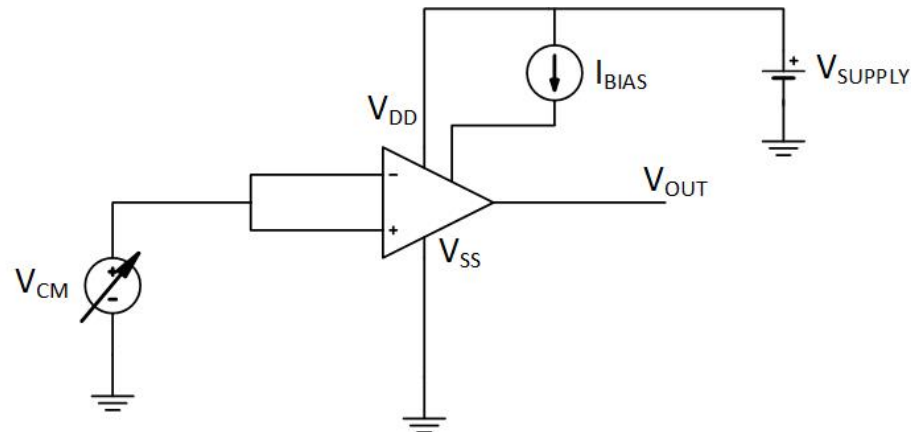


Fig 2. Setup for DC-1 testbench of OTA

- Steps for DC-2 Simulation testbench
 1. Set DC conditions of current/voltage bias for the OTA as done in DC-1 testbench
 2. Set the input common mode voltage to midpoint value of ICMR
 3. Do a DC sweep on the two inputs of OTA in differential manner with maximum/minimum voltage set by ICMR
 4. Probe the operating region of each transistors in OTA for the sweep range
 5. Range during which all transistors are in their expected region of operation will be treated as DC operating range, and the output voltage range in DC operating range will be treated as output common mode range (OCMR)

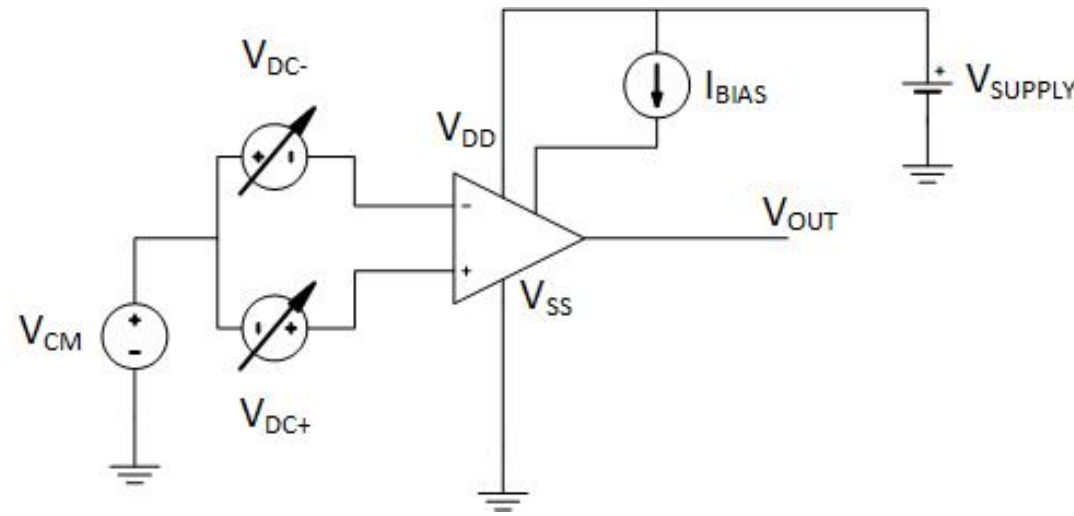


Fig 3. Setup for DC-2 testbench of OTA



Noise Testbench: Flicker Noise, Thermal Noise

- Steps for NOISE-1 Simulation testbench of OTA
 1. Setup the circuit as shown in figure given below
 2. Setup DC operating conditions using results from DC-1 simulation testbench
 3. Set the output node in noise simulation as V_{OUT}
 4. Select AC Source V_{AC} as input voltage source in noise simulation
 5. Make sure the noise models are included, and run noise simulation
 6. Plot the Input referred squared noise for flicker and thermal noise

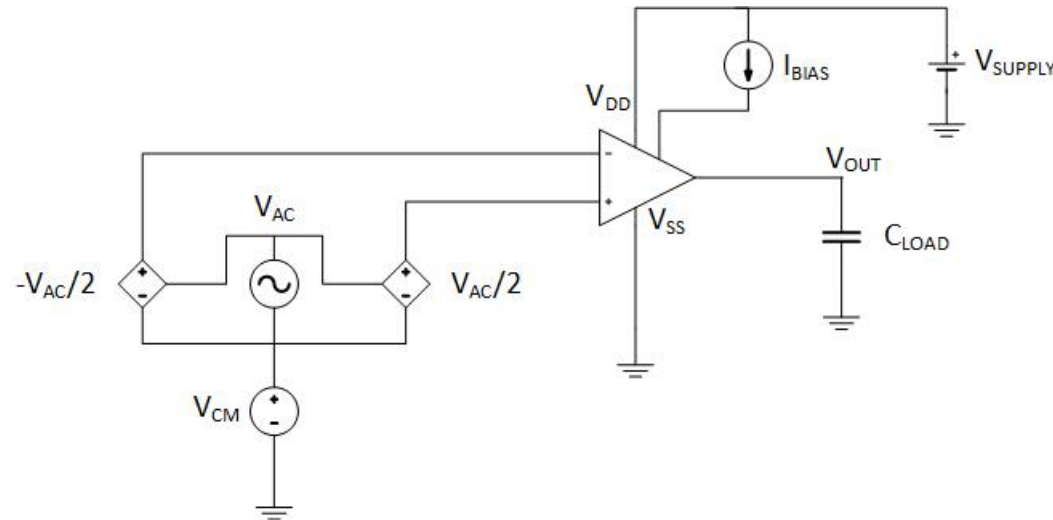


Fig 4. Setup for NOISE-1 testbench of OTA



AC Testbenches: A_{DC} , BW_{3dB} , UGF, GM, PM

- Steps for AC-1 Simulation testbench of OTA
 1. Setup DC operating conditions using results from DC simulation testbench
 2. Set the input common mode voltage to midpoint value of ICMR
 3. Add AC condition to differential inputs (AC +0.5 on positive input, and AC -0.5 on negative input terminal)
 4. Run AC simulation for frequencies f_{MIN} Hz to f_{MAX} GHz
 5. Check differential gain at f_{MIN} Hz for DC Gain (A_{DC})
 6. Subtract 3 dB from A_{DC} to get 3-dB Gain (A_{3dB}), and check the frequency at which it occurs. This frequency is the 3-dB bandwidth (BW_{3dB}).
 7. Check the frequency at which differential gain is 0 dB. This is the unity gain frequency.
 8. Check the phase response of V_{OUT} at unity gain frequency, and add this quantity with 180° to get phase margin (PM)
 9. Check the gain when phase response of V_{OUT} goes to -180° . This is the gain margin in dB.

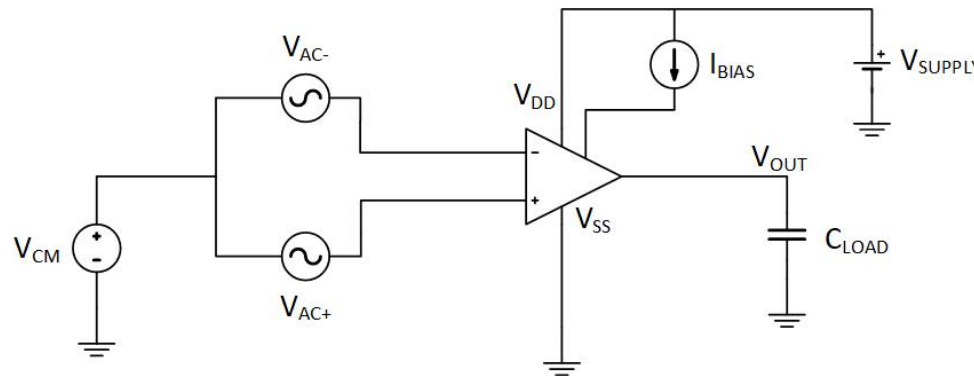


Fig 5. Setup for AC-1 testbench of OTA

- Steps for AC-2 Simulation testbench of OTA
 1. Setup DC operating conditions using results from DC-1 simulation testbench
 2. Set the input common mode voltage to midpoint value of ICMR
 3. Add AC condition to differential inputs (AC +0.5 on both - positive and negative input terminals)
 4. Add a offset voltage V_{OFFSET} to any one terminal (By default, $V_{\text{OFFSET}} = 1$ mV and is applied to positive input terminal).
 5. Run AC simulation for frequencies f_{MIN} Hz to f_{MAX} GHz
 6. Check common mode gain (A_{CM}) in dB at f_{MIN} Hz on output terminal
 7. Common Mode Rejection Ratio (CMRR) is calculated by subtracting DC Gain (A_{DC}) from common mode gain (A_{CM})

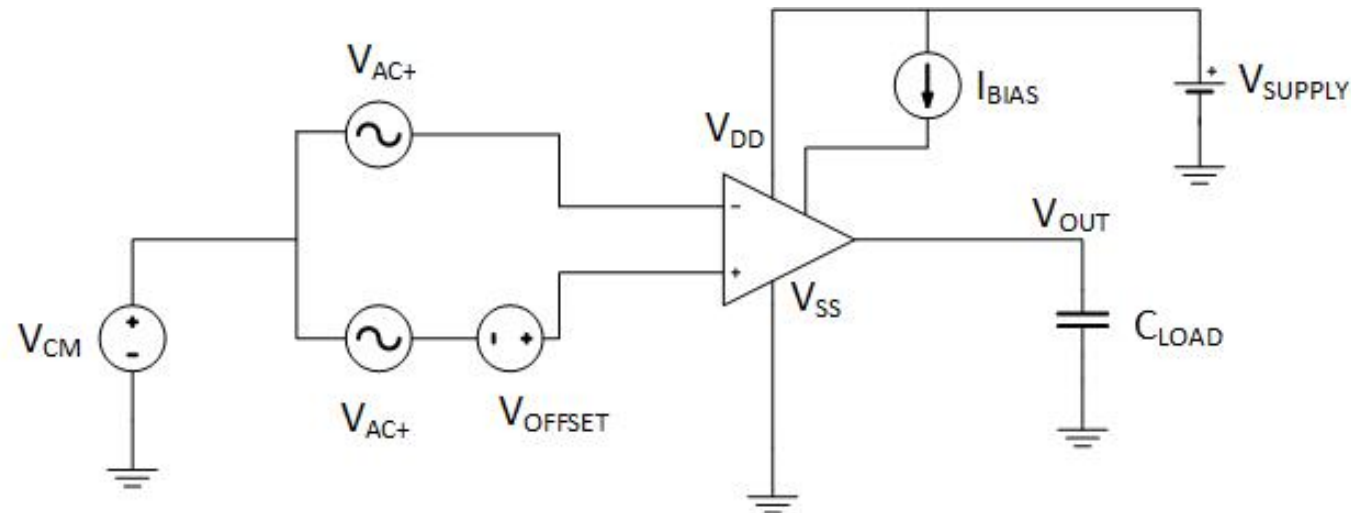


Fig 6. Setup for AC-2 testbench of OTA

- Steps for AC-3 Simulation testbench of OTA
 1. Setup DC operating conditions using results from DC-1 simulation testbench
 2. Set the input common mode voltage to midpoint value of ICMR
 3. Add AC source between supply DC source and supply pin of OTA
 4. Add a offset voltage V_{OFFSET} to any one terminal (By default, $V_{\text{OFFSET}} = 1$ mV and is applied to positive input terminal).
 5. Run AC simulation for frequencies f_{MIN} Hz to f_{MAX} GHz
 6. Check power supply gain ($A_{\text{PS+}}$) in dB at f_{MIN} Hz on output terminal
 7. Power Supply Rejection Ratio plus (PSRR+) is calculated by subtracting DC Gain (A_{DC}) from power supply gain ($A_{\text{PS+}}$)

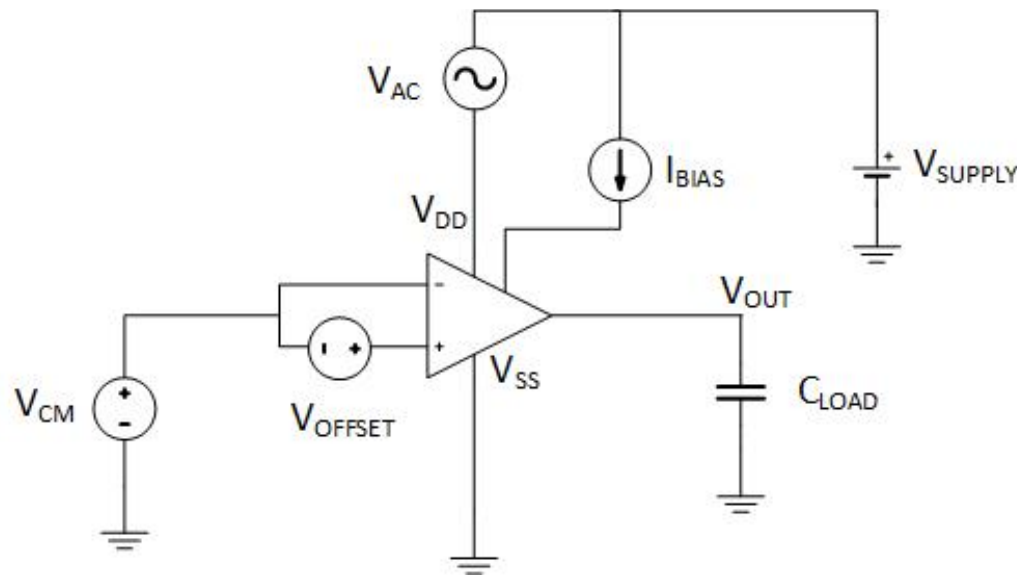


Fig 7. Setup for AC-3 testbench of OTA

- Steps for AC-4 Simulation testbench of OTA
 1. Setup DC operating conditions using results from DC-1 simulation testbench
 2. Set the input common mode voltage to midpoint value of ICMR
 3. Add AC source between ground and ground pin of OTA
 4. Add a offset voltage V_{OFFSET} to any one terminal (By default, $V_{\text{OFFSET}} = 1$ mV and is applied to positive input terminal).
 5. Run AC simulation for frequencies f_{MIN} Hz to f_{MAX} GHz
 6. Check power supply gain ($A_{\text{PS-}}$) in dB at f_{MIN} Hz on output terminal
 7. Power Supply Rejection Ratio minus (PSRR-) is calculated by subtracting DC Gain (A_{DC}) from power supply gain ($A_{\text{PS-}}$)

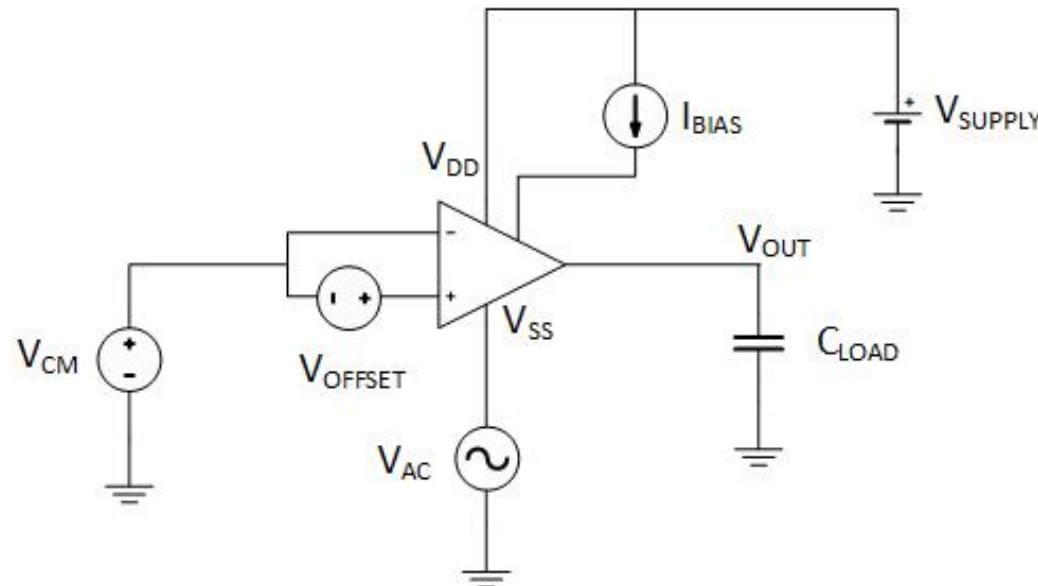


Fig 8. Setup for AC-4 testbench of OTA



TRAN Testbench: SR+,SR-

- Steps for TRAN-1 Simulation testbench of OTA
 1. Setup the circuit as shown in figure given below
 2. Setup DC operating conditions using results from DC-1 simulation testbench
 3. Set the input common mode voltage to midpoint value of ICMR
 4. Do a transient simulation by adding a PWL (Piecewise Linear) input on positive input terminal
 5. In PWL input, add a time step to move input to max ICMR, and wait till '1/UGF' time. Check the output transient
 6. Then, add a time step to move input min ICMR value, and wait till '1/UGF' time. Check the output transient
 7. Slew rate is given by rate of change of output from 10% to 90% of final settled value

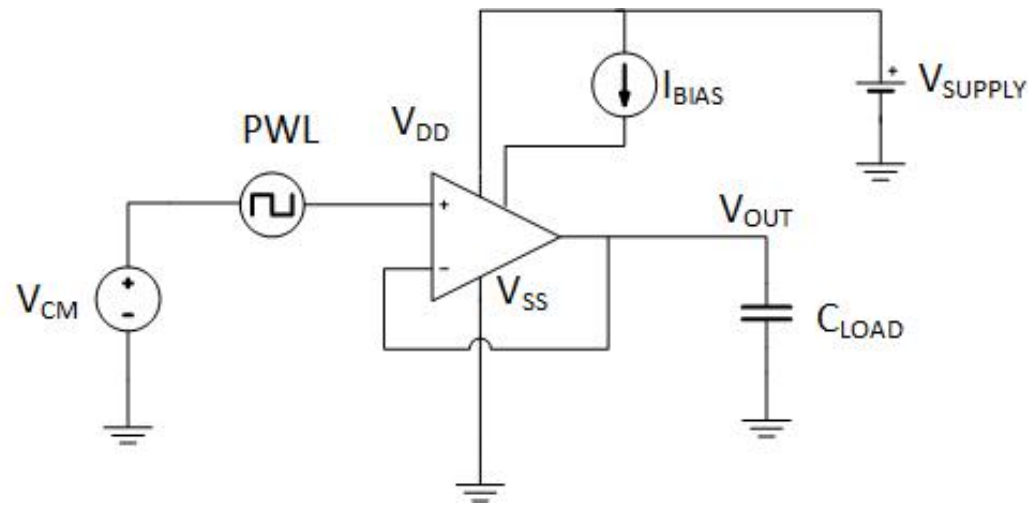


Fig 9. Setup for TRAN-1 testbench of OTA