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From WikiChip

The **14 nanometer (14 nm) lithography process** is a semiconductor manufacturing process node serving as shrink from the 22 nm process. The term "14 nm" is simply a commercial name for a generation of a certain size and its technology, as opposed to gate length or half pitch. The 14 nm node was introduced in 2014/2015 and is currently getting replaced by the 10 nm process.

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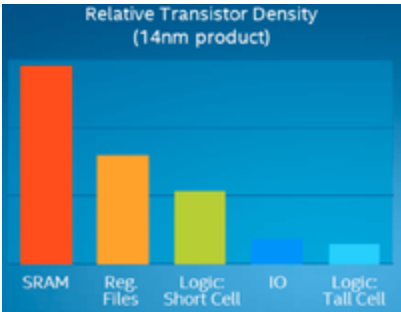
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## Industry

		Intel		Samsung Alliance		IBM (Now GlobalFoundries)		UMC	
Process Name		P1272 (CPU) / P1273 (SoC)		14LPE , 14LPP , 14LPC , 14LPU		14HP			
1st Production		2014		2015		2017		2Q 2017	
Lithography	Lithography	193 nm		193 nm		193 nm		193 nm	
	Immersion	Yes		Yes		Yes		Yes	
	Exposure	SADP		LELE		SADP			
Wafer	Type	Bulk		Bulk		SOI		Bulk	
	Size	300 mm		300 mm		300 mm		300 mm	
Transistor	Type	FinFET		FinFET		FinFET		FinFET	
	Voltage	0.70 V		0.80 V		0.80 V			
		Value	22 nm Δ	Value	20 nm Δ	Value	22 nm Δ	Value	28 n
Fin	Pitch	42 nm	0.70x	48 nm	N/A	42 nm	N/A		
	Width	8 nm	1.00x	8 nm		10 nm			
	Height	42 nm	1.24x	37 nm		25 nm			
Gate Length (L <sub>g</sub> )		20 nm	0.77x	30 nm		18-26 nm	0.72-0.79x		
Contacted Gate Pitch (CPP)		70 nm	0.78x	78 nm	1.22x	80 nm	0.80x		
Minimum Metal Pitch (MMP)		52 nm	0.65x	64 nm	1.00x	64 nm	0.80x		
SRAM bitcell	High-Perf (HP)	0.0706 μm <sup>2</sup>	0.54x	0.080 μm <sup>2</sup>	0.78x	0.0900 μm <sup>2</sup>	0.63x		
	High-Density (HD)	0.0499 μm <sup>2</sup>	0.54x	0.064 μm <sup>2</sup>	0.79x	0.0810 μm <sup>2</sup>	0.81x		
	Low-Voltage (LV)	0.0588 μm <sup>2</sup>	0.54x						
DRAM bitcell	eDRAM					0.0174 μm <sup>2</sup>	0.67x		

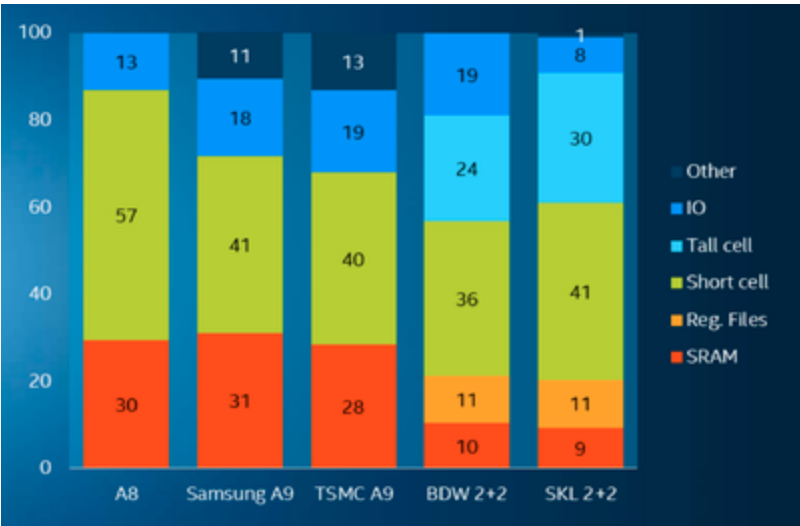
## Composition

It's important to note that not all processes compete with each other. The process should cater to the products that will make use of the underlying technology. The composition of the actual integrated circuit also varies by manufacturer and by design due to different goals. For example, the cache on Apple's 14 nm A9 (manufactured by Samsung) accounts almost 1/3 of the entire chip whereas Intel's Broadwell cache accounts for only 10% of



the entire chip. Likewise, Intel's Broadwell and Skylake target high-performance and incorporate a large amount of higher-speed elements which are inherently sparse. Tall cells account for almost 30% Skylake's composition and less than 1% on Apple's A8 or A9.

Those numbers are somewhat expected given tall logic cells are generally optimized for performance and high frequency (e.g., high-switching circuitry in the CPU) whereas short cells are optimized for density (e.g., GPU shader arrays).



It should be noted that SRAM is the densest component of the process in a chip, with sometimes up to three or four times the density of logic cells that are used in the same process. It should be noted that in recent years, SRAM hasn't scaled as well as logic and I/O have either.

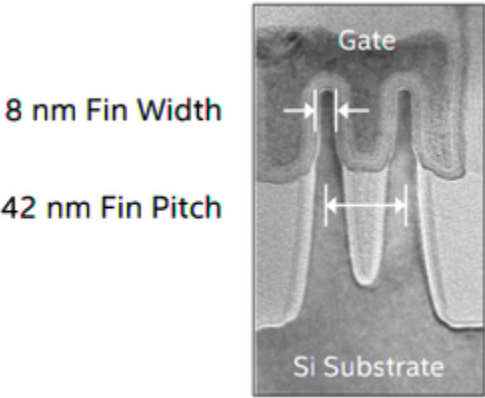
Intel

See also: Intel's Process Technology History

Intel got off to a bumpy start with major yield problems initially, but by Skylake yield has reached very healthy numbers. 14 nm became Intel's 2nd generation FinFET transistors. Intel uses TiN pMOS / TiAlN nMOS as work function metals. Intel makes use of 193 nm immersion lithography with Self-Aligned Double Patterning (SADP) at the critical patterning layers. Compared to all other "14 nm nodes", Intel's process is the densest and considerably so, with >1.5x raw logic density.

Intel's 14 nm process has gone through multiple refinements optimizing higher clock speed, higher drive current, and lower power dissipation. The original "14nm" was used for their Broadwell and mainstream Skylake processors. They improved on their original process with a second process, "14nm+", offering 12% higher drive current at lower power. That process has been used for both Kaby Lake and Server/HEDT Skylake SP/X processors.

A third improved process, "14nm++", is set to begin in late 2017 and will further allow for +23-24% higher drive current for 52% less power vs the original 14nm process. The 14nm++ process also appear to have slightly relaxed poly pitch of 84 nm (from 70 nm). It's unknown what impact, if any, this will have on the density.

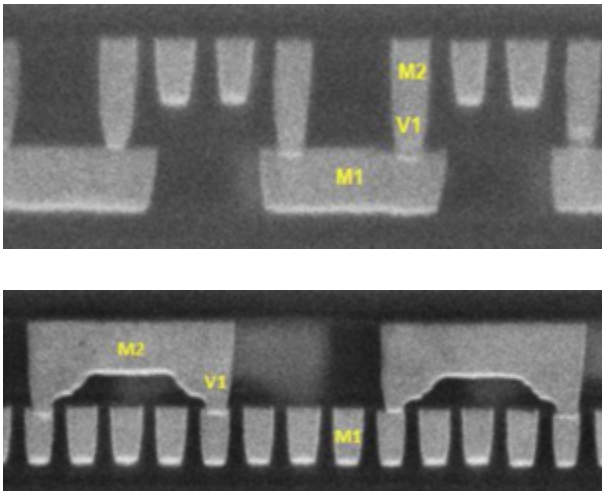


Intel 14nm Design Rules

[show]

IBM

IBM developed their own "14HP" (14nm High-Performance) process at their East Fishkill, NY plant. Note that the plant AND the process, along with numerous semiconductor technology IPs, were sold to GlobalFoundries in late 2014. GF still operates the plant (also by ex-IBM semiconductor engineers) and the process which is used by IBM for their various processors. This process was designed by IBM for their very large chips with effective power supply and clock distribution capable of producing dies as large as 700 mm<sup>2</sup> and larger with a hierarchical BEOL of 17 levels of copper interconnect for high performance wire-ability. It should be noted that GlobalFoundries had no such capabilities prior to their acquisition of IBM's plant, semiconductor manufacturing group, and IP portfolio.



IBM's HP 14nm CMOS process features a FinFET architecture on an SOI substrate. The use of SOI with FinFET gives IBM a number of unique advantages such as lower parasitic capacitance at the base of the fin as well as simplifies patterning of the active fins and minimizes their variability such as height and thickness. The architecture also includes high-density deep-trench embedded DRAM cells with a reported size of 0.0174 μm<sup>2</sup>. The process features an L<sub>gate</sub> of 20nm and smaller (18nm to 27nm) which IBM reported to result in over 35% performance gain verses their HP 22nm process (for identical V<sub>dd</sub> = 0.80 V).

IBM 14nm Design Rules		[hide]
Layer	Pitch	
Fin	42 nm	
Contacted Gate Pitch	80 nm	
Metal 1	64 nm	
Metal 2	80 nm	
Metal 3	128 nm	
Metal 4	256 nm	
Metal 5	512 nm	
Metal 6	2.56 μm	

Samsung

This process became Samsung's and GlobalFoundries first generation of FinFET-based transistors. Samsung uses TiN pMOS / TiAIC nMOS as work function metals. Samsung node has gone through a number of refinements from 14LPE (14 Low-Power Early) to 14LPP (14 Low-Power Performance) and further.

In late 2017, Samsung announced "11LPP" (11 Low-Power Plus) which is a further enhancement of 14LPP. 11LPP is reported to deliver up to 15% higher performance with enhanced design rules that allow for up to

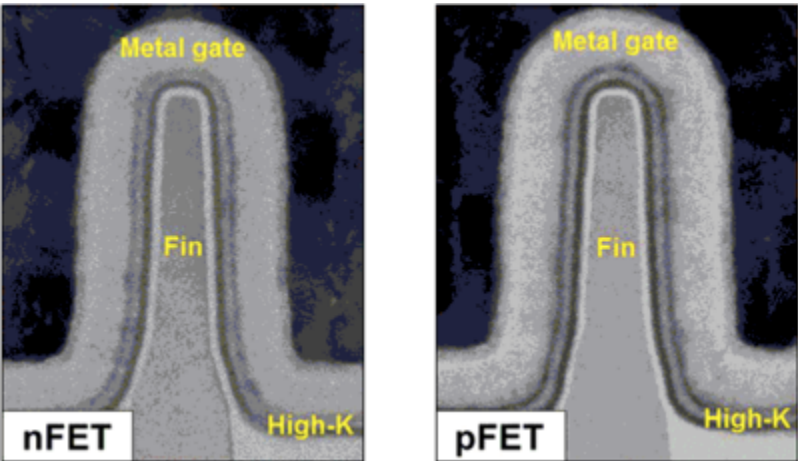
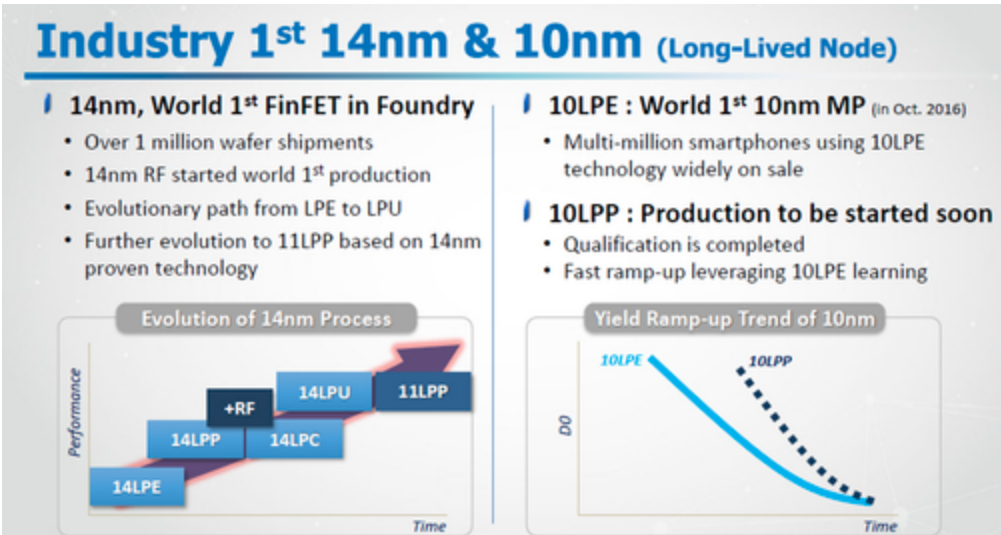
10% reduction in area. Samsung expects 11LPP to enter mass production in late 2017 or early 2018.

**GlobalFoundries**

Building on top of Samsung's licensed 14nm process, GlobalFoundries announced the "12LP" (12 nm Leading Performance) process in late 2017 which is said to deliver up to 15% increase in density and 10% increase in performance through further cell optimization such as track reduction.

**UMC**

UMC announced the start of 14nm process mass production in February 2017. The 14nm process is their first process to use FinFET, and provides up to 55% higher performance and twice the gate density compared to their 28nm process.



**Find models**

Click to browse all 14 nm MPU models

**14 nm Microprocessors**

- AMD

- EPYC
  - EPYC Embedded
  - Ryzen 3
  - Ryzen 5
  - Ryzen 7
  - Ryzen Embedded
  - Ryzen Threadripper
- 
- Apple
    - Ax
  - Intel

- Atom x5
- Atom x7
- Core i3
- Core i5
- Core i7
- Core i7EE
- Pentium
- Pentium Gold
- Pentium Silver
- Celeron
- Xeon
- Xeon Bronze
- Xeon D
- Xeon E3
- Xeon E5
- Xeon E7
- Xeon Gold
- Xeon Platinum
- Xeon Silver

- Samsung
  - Exynos

*This list is incomplete; you can help by expanding it ([https://en.wikichip.org/w/index.php?title=14\\_nm\\_lithography\\_process&action=edit](https://en.wikichip.org/w/index.php?title=14_nm_lithography_process&action=edit)).*

## 14 nm Microarchitectures

- Intel
  - Airmont
  - Goldmont
  - Broadwell
  - Skylake
  - Kaby Lake
  - Coffee Lake
  - Whiskey Lake

- Amber Lake
- Comet Lake
- Cascade Lake
- Cooper Lake
- AMD
  - Zen
  - Zen refresh
  - Arctic Islands
  - Vega
- IBM
  - POWER9
  - z14
- Samsung
  - Mongoose 1

*This list is incomplete; you can help by expanding it (<https://en.wikichip.org>*

*/w/index.php?title=14\_nm\_lithography\_process&action=edit).*

## Documents

- Intel's 14 nm Technology: Delivering Ultrafast, Energy-Sipping Products
- Intel's 14nm, Advancing Moore's Law, investor meeting
- Intel's 14 nm technology leadership, Dr. Ruth Brain

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Category: lithography

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