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Application Note

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Understanding the 16-bit ADC PGA in Kinetis K series

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1 Introduction

Freescale's Kinetis microcontrollers integrate a 16-bit analog-to-digital converter (ADC16) with built-in programmable gain amplifier (PGA), which is capable to operate in several modes.

The Programmable Gain Amplifier (PGA) is designed to increase the dynamic range by amplifying low-amplitude signals before they are fed to the 16-bit ADC.

1.1 Abstract

Whenever a gain stage is included in the converter path, the Signal to Noise Ratio (SNR) will go down. This effect occurs because the PGA induces noise into the system. Therefore, question may arise why would an application include PGA on the system?

The main reason to include a PGA stage before an ADC conversion is to increase the dynamic range. Dynamic range indicates the minimum resolvable step size and the ratio between the largest and smallest possible inputs. Resolution is the number of bits in the result, and is often confused with dynamic range.

1.2 Objective

This document describes technical observations and transfer functions of the ADC16 and ADC16-PGA measurement chains in typical measurement use-cases. The information provided in this application note has been validated by experimental measurements on TWR-K60N512 board.

2 Kinetis PGA integration

Kinetis K series 72 MHz and 100 MHz microcontrollers feature up to two 16-bit ADCs. Each ADC contains a PGA channel for a total of two separate PGAs as shown in Figure 1.

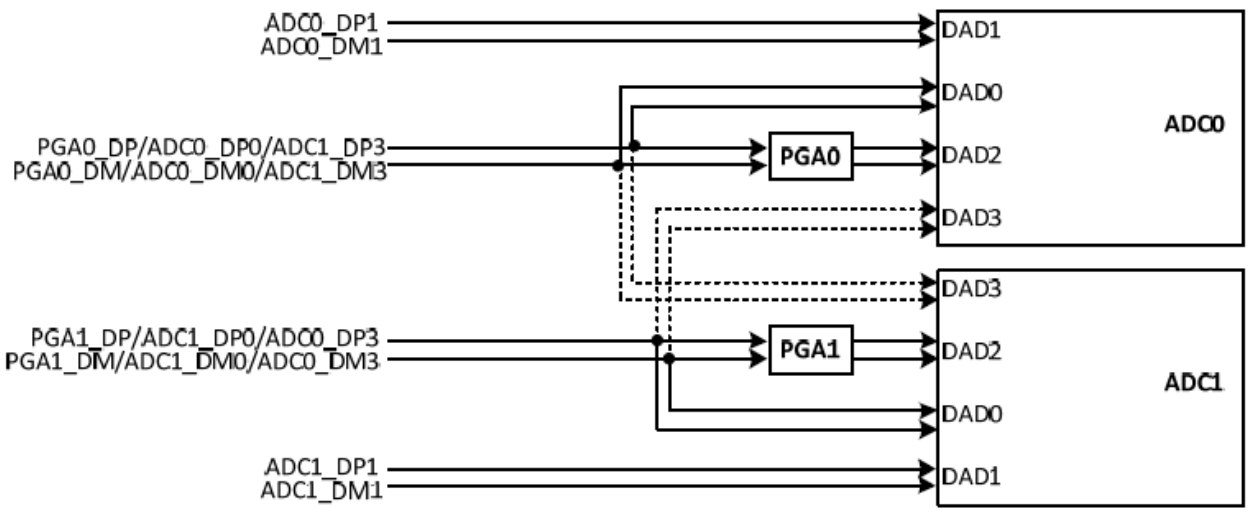

Figure 1. Dual ADC PGA integration

Kinetis K series120 MHz and 150 MHz have up to four ADCs. Each ADC contains a PGA channel for a total of four separate PGAs as shown in Figure 2.

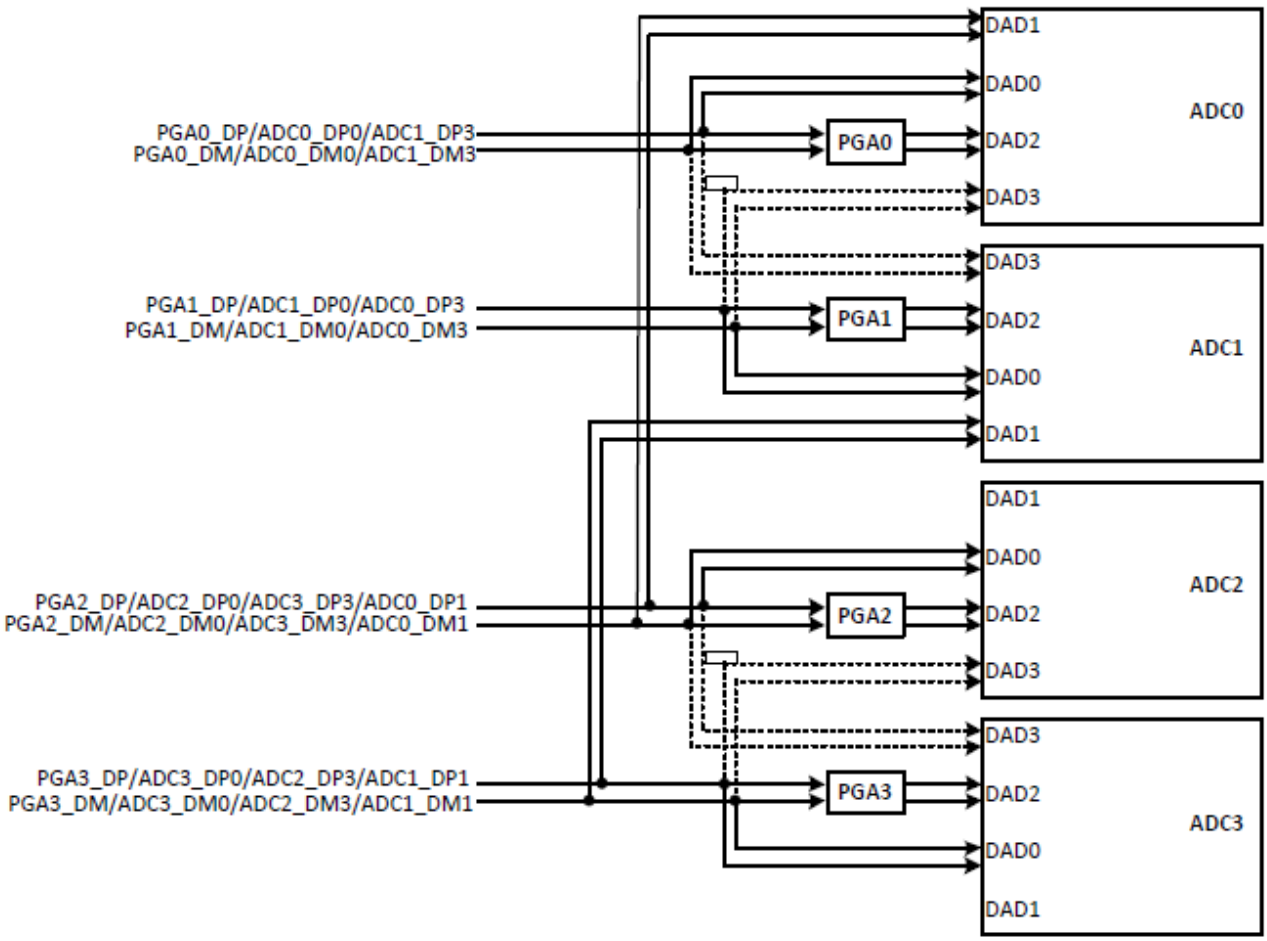

Figure 2. Quad ADC PGA integration

2.1 PGA voltage range

PGA reference option is the only 1.2 V V $_{REF\_OUT}$ source. The V_{REF_OUT} signal can either be driven by an external voltage source[1] via the V_{REF_OUT} pin or from the output of the VREF module.

The PGA differential mode operation takes a differential input voltage. ADC results will be the amplified difference between PGA Differential Plus (PGA_DP) and PGA Differential Minus (PGA_DM) with the common mode correction.

Eqn. 1 shows that the PGA common mode voltage[2], V_x, is set to 700 mV

$$V_x = V_{REF} \times 0.583 \qquad \text{Eqn. 1}$$

The formula at Eqn. 2 describes the maximum PGA differential input signal swing[3] for the ADC16-PGA

1. Ensure that the VREF module is disabled when an external voltage is used (applied at the V_{REF_OUT} pin) instead of the VREF module.
2. The expected variations of the PGA common mode voltage are in the range +–15–20 mV. Those variations are caused by PGA common mode control circuit. The increase of common mode voltage causes decrease of the maximum differential input swing, expressed by Eqn. 2

$$V_{ppADC,DIF} = \frac{\min\left(V_x - 0.2, V_{VREF} - V_x\right) \times 4}{\text{Gain}} \quad \text{Eqn. 2}$$

where: V_x is 700 mV

$V_{VREF}$is 1.2 V

Gain represents the possible PGA gains (1, 2, 4, 8, 16, 32, 64)

Theoretically,16-bit ADC digital output range can be calculated by

$$ADC_{OUT} = \left(\frac{V_{ppADC,DIF}}{2 \times V_{VREF}}\right) \times Gain \times 2^N \quad \text{Eqn. 3}$$

where:N is the number of bits (resolution) selected for the current conversion

PGA_DP and PGA_DM peak-to-peak maximum permitted voltages

$$V_{ppDP,ppDM} = \frac{V_{ppADC,DIF}}{2} \quad \text{Eqn. 4}$$

where: $V_{ppDP,ppDM}$ is the peak-to-peak voltage at the PGA inputs

$V_{PPADC,DIF}$ is the peak-to-peak PGA differential input swing

V_{ppDP} is the maximum peak-to-peak voltage at the PGA plus-side input pin

V_{ppDM} is the maximum peak-to-peak voltage at the PGA minus-side input pin

$_{VREFPGA}$ is the PGA voltage reference (V_{REF_OUT})

Table 1 summarizes differential input signal swing and respective digital output range of the ADC16 for all PGA gain stages.

Table 1. PGA input ranges

PGA Gain	$V_{PPADC,DIF}$	ADC_{OUT}
× 01	2000 mV	54613 LSB
× 02	1000 mV	
× 04	500 mV	
× 08	250 mV	
× 16	125 mV	
× 32	62.5 mV	
× 64	31.25 mV	

3. Formula describes maximum differential input swing taking into account the overall ADC16-PGA measurement chain. Note that it differs from datasheet formula, $V_{PPADC,DIF}$=((min(V_x,V_{DDA} – V_x) – 0.2) ×4)/*Gain*, which expresses PGA maximum differential input swing.

3 PGA dynamic input examples

The following sections show the maximum differential input swing of the ADC16-PGA measurement chain using two different PGA gain stage settings. For the first, PGA gain is set to one (x1), then measurement is made with PGA gain set to the maximum gain (x64).

3.1 PGA enable (gain = 01)

A differential 2000 mVpp sinusoidal signal is applied on the positive (PGA_DP) and negative (PGA_DM) inputs of the PGA. Both ADC16 and PGA have been set to 1.2 V reference driven by the internal VREF module (measured reference voltage 1.1972 V). When the PGA gain is set to 1, the experiment shows what is in Figure 3.

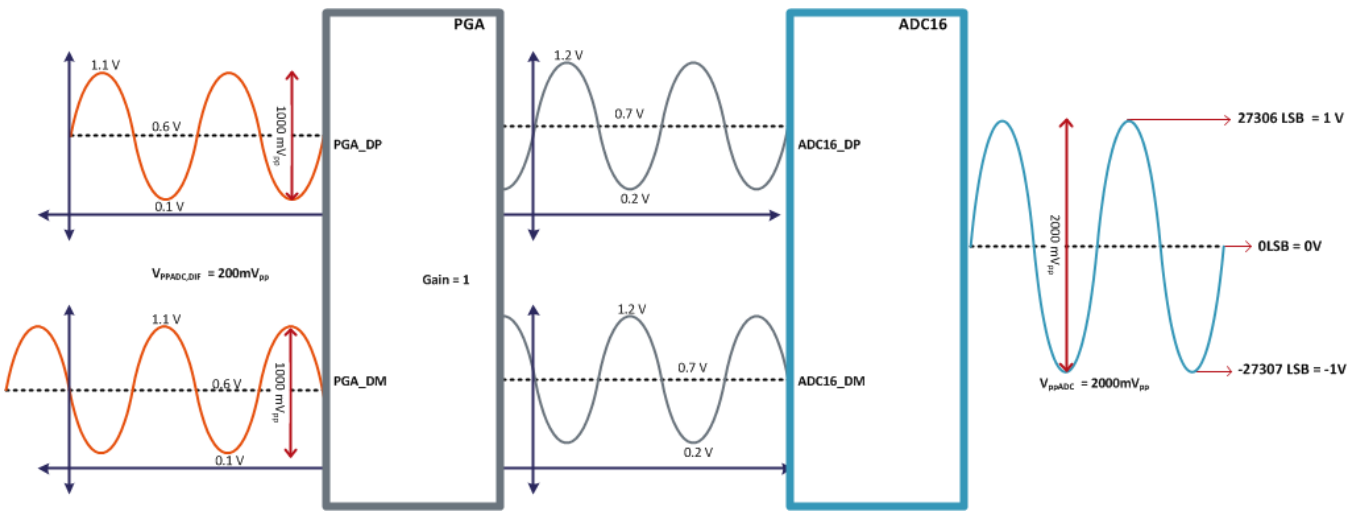

Figure 3. Differential input waveform setup (PGA enable, gain = 01)

At the PGA output, the common voltage is switched to 700 mV. Because the inputs are always corrected to the PGA common voltage, it does not matter if PGA_DP and PGA_DM go above 1.2 V, as long as the signal swing is inside the permitted value as shown in Table 1.

The ADC16 output range for differential sine waveform input 2000 mVpp PGA gain of 1 is shown in Figure 4.

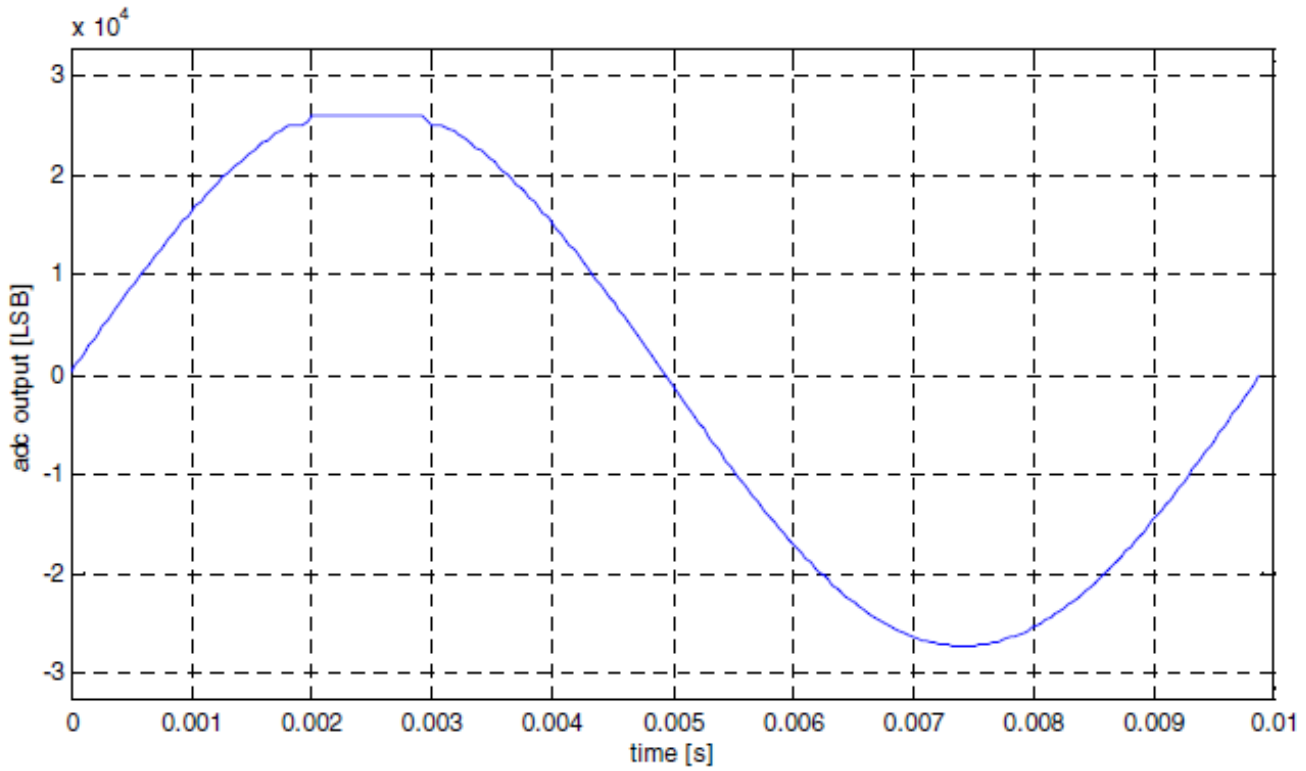

Figure 4. Digital output range at full input swing (PGA enable, gain = 01)

The range of the ADC digital output codes is 53369 LSB. It is close to the expected digital output range (54613 LSB) given in Table 1.

3.2 PGA enable (gain = 64)

A differential 31.25 mVpp sinusoidal signal has been applied on the positive and negative inputs of the PGA. Both ADC16 and PGA have been set to 1.2 V reference driven by the internal VREF module (measured reference voltage 1.1972 V). The PGA gain was set to 64. The experiment setup is shown in Figure 5.

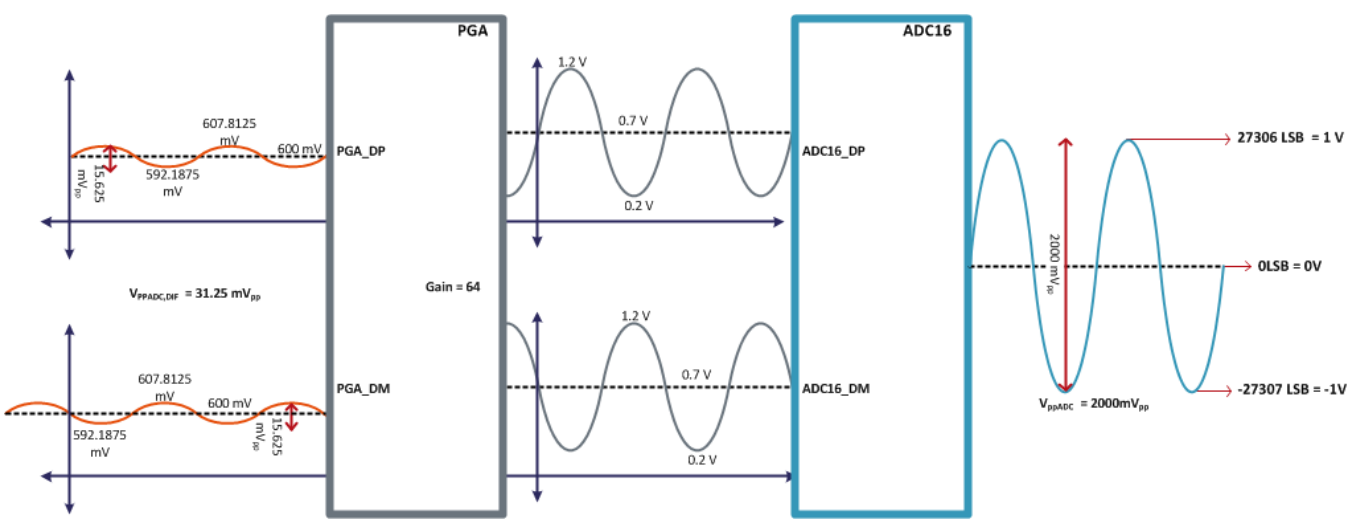

Figure 5. Differential input waveform setup (PGA enable, gain = 64)

The ADC16 output range for differential sine waveform input 31.25 mVpp PGA gain of 64 is shown in Figure 6.

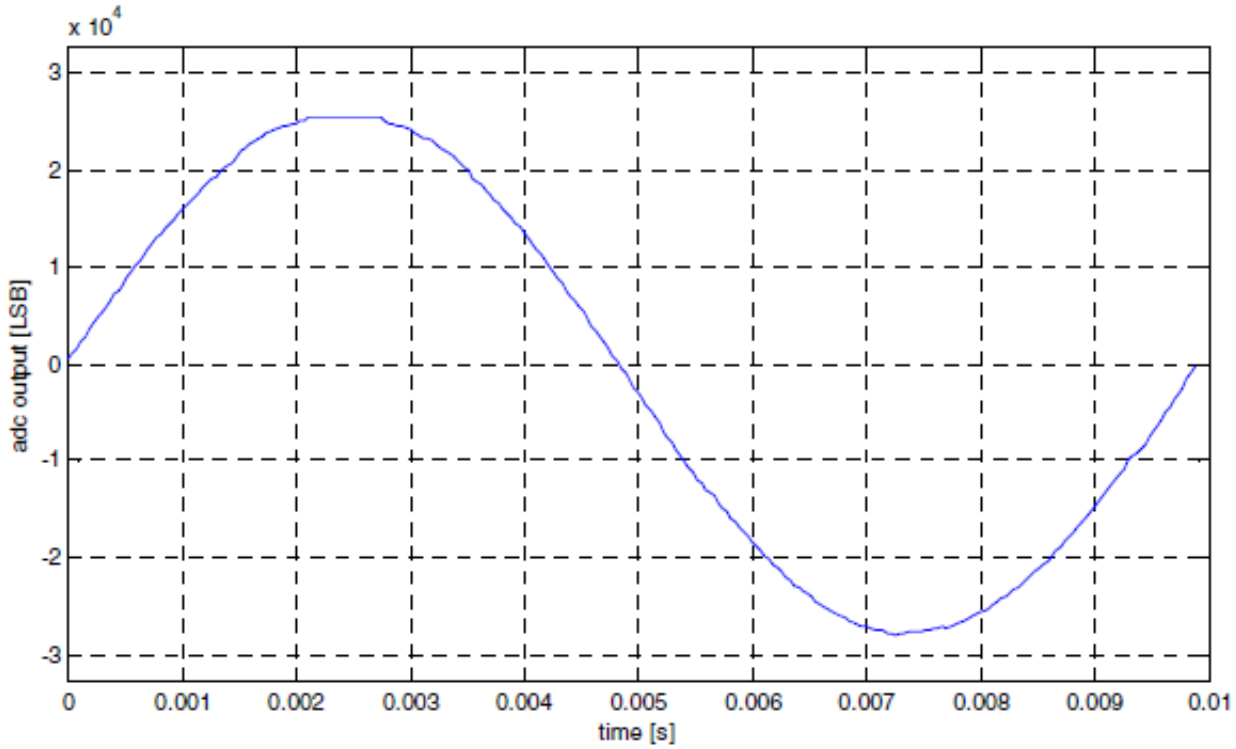

Figure 6. Digital output range at full input swing (PGA enable, gain = 64)

The ADC digital output code range measured on the ADC is 53489 LSB, which is close to the theoretical range of 54613 LSB shown in Table 1.

4 16-bit ADC measurement use-case

This section shows typical ADC16 differential measurement use-casewith PGA disable. The purpose of this experiment is to show the tradeoffs between ADC16 differential measurements and PGA-ADC16 conversions.

Figure 7 shows a differential 2400 mVpp sinusoidal signal applied to an ADC16 differential inputs with PGA bypassed. The ADC16 voltage reference is set to 1.2 V driven by the internal VREF module (measured reference voltage 1.1972 V)

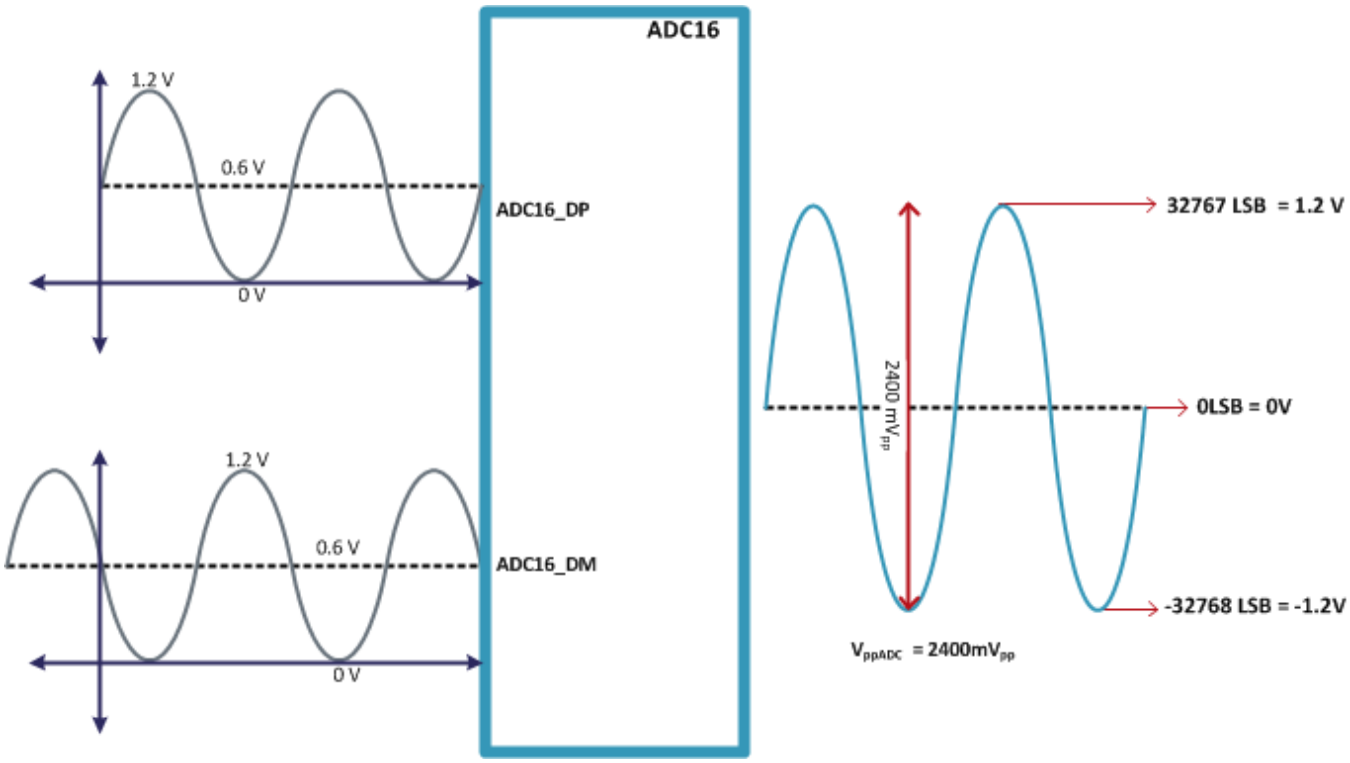

Figure 7. Differential input waveform setup (PGA disable)

The ADC16 output range for differential sine waveform input 2.4 Vpp is shown in Figure 8.

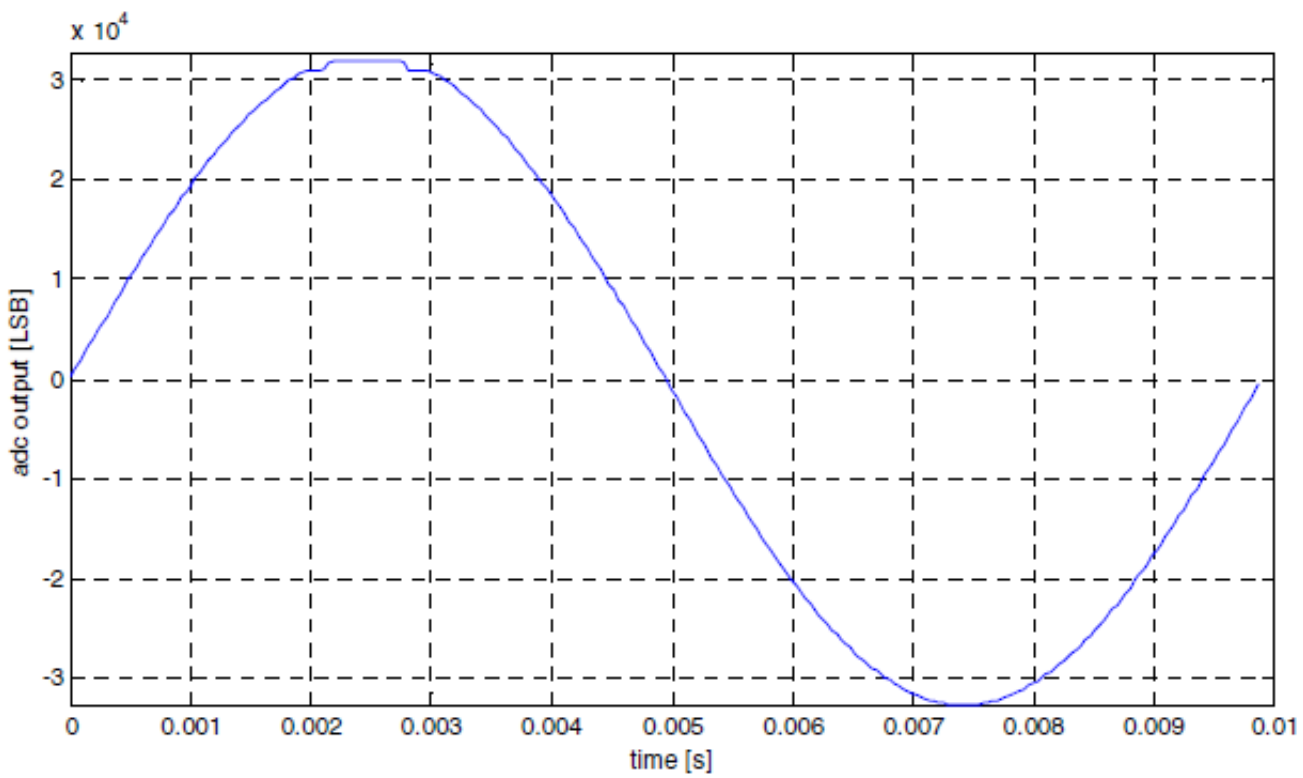

Figure 8. Digital output range at full input swing (PGA disable)

The ADC digital output code range measured on the ADC is 64753 LSB, which is close to the theoretical range of 65536 LSB shown in Table 1.

5 Conclusion

The comparison of input signal swings and maximum digital output ranges of typical ADC16 measurement use-cases has been performed.

When amplifiers are used the application needs to take into account that there are no ideal responses, accuracy lost or error will always be present. Kinetis PGA has a common mode voltage reference different to the ideal VREF/2 and there is also an offset error VOFS.

Therefore, the theoretical input swing is higher when PGA is disabled – see Table 2 (bold entries). Although ADC16 with PGA disabled increases the input swing, dynamic range will always be the same because there is no pre-amplification stage.

Table 2. PGA impact on 16-bit ADC input voltage range

Use-Case	$V_{PPADC,DIF}$	Theoretical ADC_{OUT}	Measure ADC_{OUT}
ADC16-PGA MEASUREMENT (PGA enabled, gain=x64)	31.25 mVpp	54613 LSB	53489 LSB
ADC16-PGA MEASUREMENT (PGA enabled, gain=x01)	**2000 mVpp**	**54613 LSB**	53369 LSB
ADC16 MEASUREMENT (PGA disabled)	**2400 mVpp**	**65536 LSB**	64753 LSB

Conversion results, obtained from ADC16 result registers, shown at Figure 4, Figure 6, and Figure 8 show difference between theoretical and measurement values. ADC16 results in conversion error when positive input is near upper rail reference voltage. It occurs only in 16-bit differential mode while other modes of operation are unaffected. Such behavior of the analog converter, its root cause and workaround is known and described under errata e3863[4]. The conversion error attributed to given errata can be considered as the deviation between "ADC_{OUT} Theoretical" and "ADC_{OUT} Measure" – see Table 2.

6 References

Freescale's "KINETIS_4N30D - Mask Set Errata for Mask 4N30D", Rev.15 MAY 2012, available in freescale.com

4. Freescale's "KINETIS_4N30D - Mask Set Errata for Mask 4N30D", Rev.15 MAY 2012, freescale.com

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