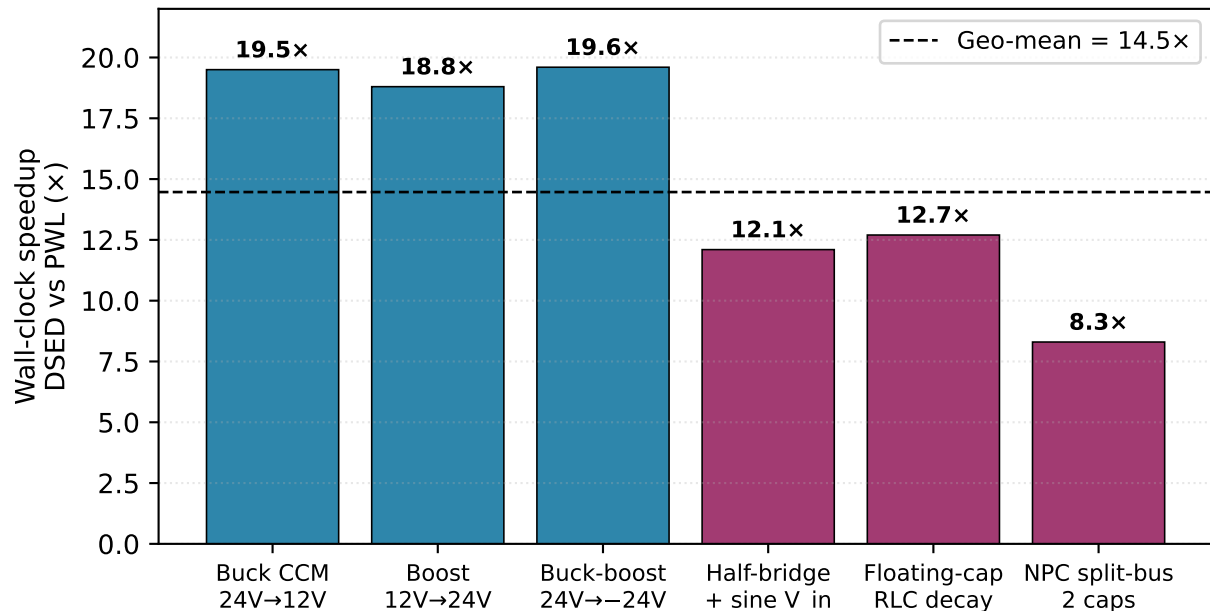


DSED (engine='dsed', native) vs PWL (engine='pwl', fixed-step trap) — buck CCM headline 24x

DSED ÷ PWL across 6 converter topologies



Where the speedup comes from: fewer steps

